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# Chapter 1

## Introduction and Overview

This document is intended to provide a detailed summary of the North American custom electronics for the  $G^0$  experiment. Only information about this subsystem will be provided here. General information about the experiment and other subsystems may be found elsewhere.

Figure 1.1 shows a block diagram of the  $G^0$  electronics for the forward angle running and figure 1.2 shows the block diagram for the backward angle running. The custom made electronics are shown as dark boxes.

The document is divided into chapters, one for each custom electronics module. Each chapter will give a detailed description of the electronics module including function, inputs and outputs, power and crate requirements, front panel layout, and printed circuit board layout.

Chapters 2 and 3 will discuss the Splitter and Meantimer modules. The Constant Fraction Discriminators (CFDs) will be discussed in chapter 11, Commercial Electronics. Chapters 4 and 5 will discuss the Clock Gating Board (KGB) and the Signal Distribution Board (SDB) which are used to form and distribute the gated clock and SYNC pulses to the Latching Time Digitizer (LTD) boards. Chapter 6 will cover the LTD boards. Chapter 7 will describe the Munger modules, which reorganize the LTD time bits for input to the scalars. The scalars will be discussed in chapter 11. Chapters 8 and 9 will discuss the CEBAF and DADDY boards respectively. These boards were developed for testing of the LTDs.

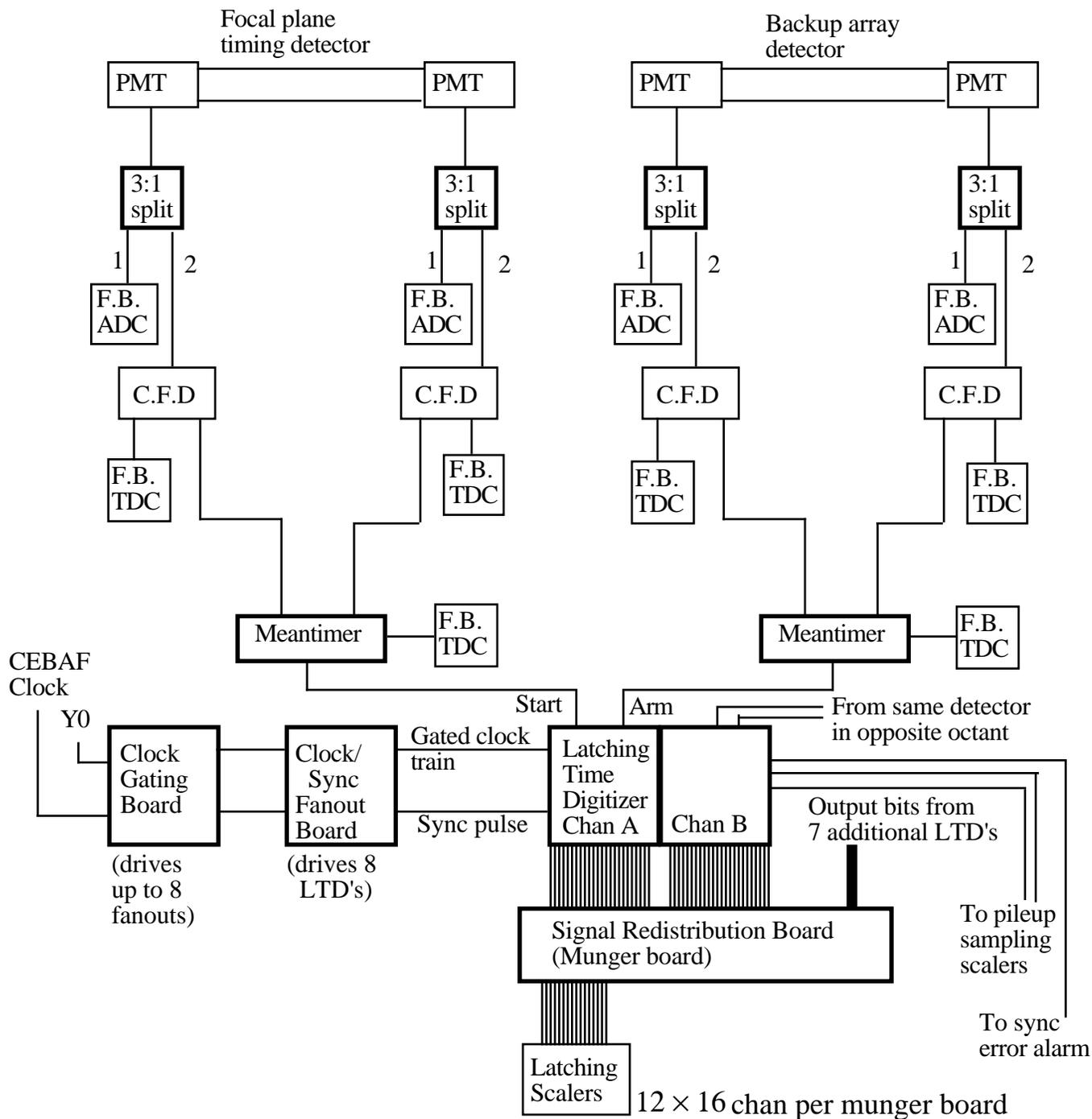


Figure 1.1: Electronics block diagram for the forward-angle (proton detection) running mode. Custom electronics are shown as dark boxes.

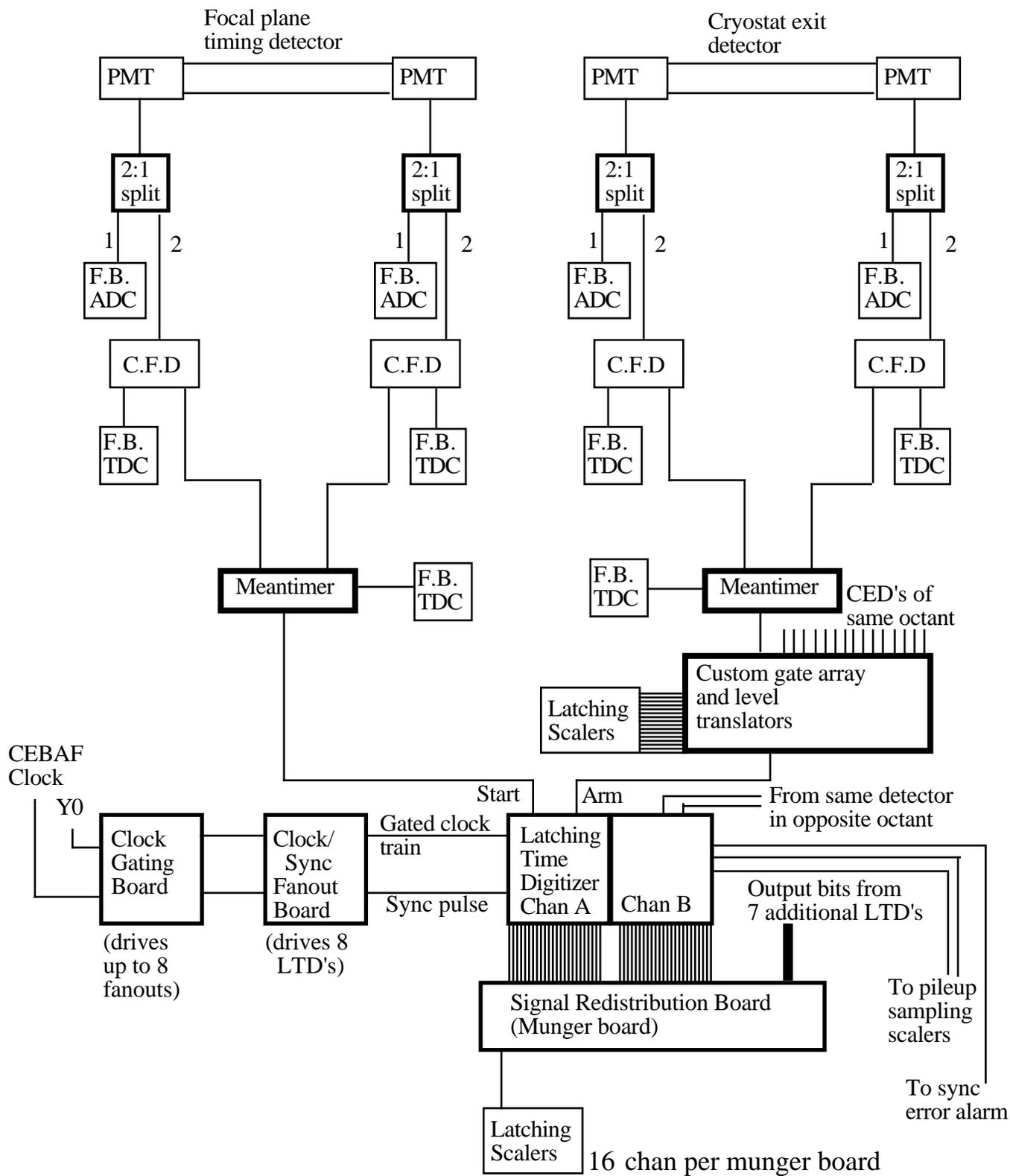


Figure 1.2: Electronics block diagram for the backward-angle (electron detection) running mode. Custom electronics are shown as dark boxes.

# Chapter 2

## Splitter Modules

### 2.1 Function

The Splitter module asymmetrically (70:30) splits the PMT signals to provide inputs for the CFDs and FASTBUS ADCs. The input impedance is  $50 \Omega$ , the CFD output back impedance is  $50 \Omega$  and the ADC output back impedance is  $110 \Omega$ . Figure 2.1 shows a schematic of a single Splitter channel. The split is passive so the module does not require power.

### 2.2 Inputs and Outputs

The Splitter has 32 BNC input connectors on the back side of the module. The module is 1 U high and the BNC connectors are set in two horizontal rows. They are arranged in two groups of 16, each group being numbered from 1 to 16. The first group is composed of the top and bottom rows on the right (as viewed from the front) and the second group is on the left. Figure 2.1 shows the layout of the connectors on the back panel. On the front side of the module, there are two 34 pin ribbon cable connectors for the ADC signals. One on the right corresponds to the right set of 16 BNC inputs and the one on the left corresponds to the left set of 16 BNC connectors. There are also two bundled coaxial cables on the front which are for the CFD signals. Each bundle has 16 coaxial lines and is terminated with a 34 pin connector. As with the ribbon connectors, the bundled cable on the right corresponds to the right set of 16 BNC connectors and the left bundled cable corresponds to the left set of 16 BNC connectors. Table 2.1 lists the output pins for the CFD and ADC signals on the right side with the left being identical. Within the splitter module there are two printed circuit boards, one for the right side of connectors and one for

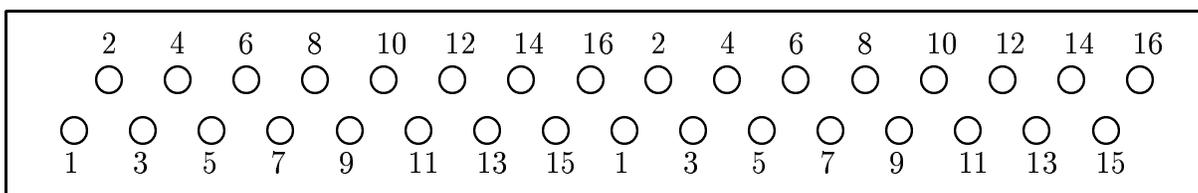


Figure 2.1: Back panel layout of Splitter module.

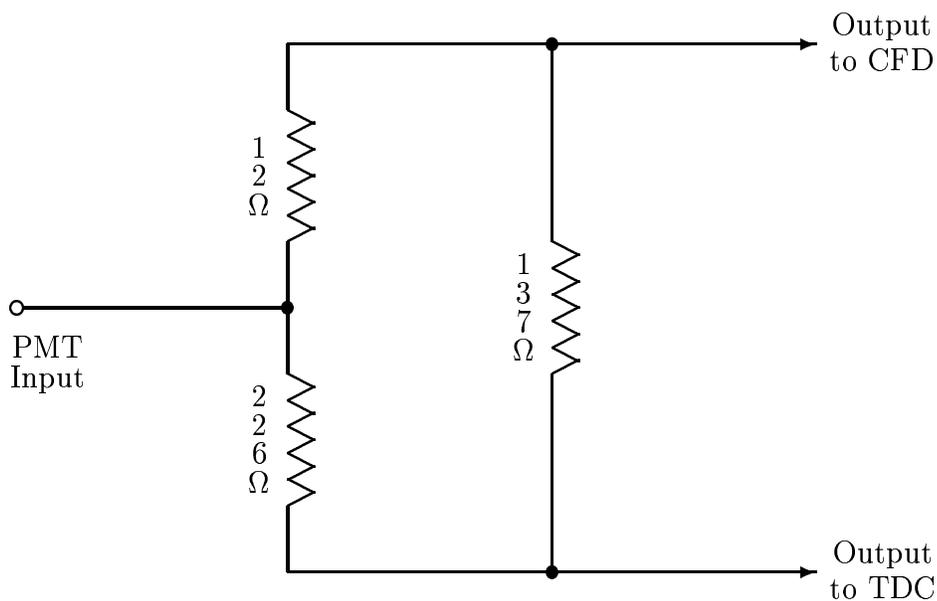


Figure 2.2: Schematic of a single Splitter channel.

the left. The two printed circuit boards are identical. The layout of the boards is shown in figure 2.1.

## 2.3 Module Construction

Figure 2.3 shows the layout of the splitter two layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the splitter module is given in table 2.3.

Output	Connector	Input
1 (right)	CFD, ADC	1 BNC (right)
2 (right)	CFD, ADC	2 BNC (right)
3 (right)	CFD, ADC	3 BNC (right)
4 (right)	CFD, ADC	4 BNC (right)
5 (right)	CFD, ADC	5 BNC (right)
6 (right)	CFD, ADC	6 BNC (right)
7 (right)	CFD, ADC	7 BNC (right)
8 (right)	CFD, ADC	8 BNC (right)
9 (right)	CFD, ADC	9 BNC (right)
10 (right)	CFD, ADC	10 BNC (right)
11 (right)	CFD, ADC	11 BNC (right)
12 (right)	CFD, ADC	12 BNC (right)
13 (right)	CFD, ADC	13 BNC (right)
14 (right)	CFD, ADC	14 BNC (right)
15 (right)	CFD, ADC	15 BNC (right)
16 (right)	CFD, ADC	16 BNC (right)

Table 2.1: Outputs for the Splitter Module. The outputs for the CFD and ADC are on the back of the module, while the BNC inputs are on the front. Right and left here refer to the module as viewed from the front. Both the CFD and ADC output connectors have the same pin configuration, so both are listed together. Likewise, right and left are identical so only the right is listed.

Quan.	Description	Manufacturer	Part Number
	High temp. coaxial cable 500 ft.	Belden	83269-500-9
1	13 inch rack mount cabinet	Bud Indus.	NHC-14152
2	34 pin male RA DIN con.	FCI	71922-134
2	34 pin Molex con.	Molex	22-55-2341-P
32	BNC bulkhead con.	Amphenol	31-10
32	12.4 $\Omega$ resistor	Yageo	MFR-25FBB-12R4
32	137 $\Omega$ resistor	Yageo	MFR-25FBB-137R
32	226 $\Omega$ resistor	Yageo	MFR-25FBB-226R

Table 2.2: Parts List for Splitter

Figure 2.3: Layout of the Splitter board (SPLITTER.BD1).

# Chapter 3

## NIM Meantimer Modules

### 3.1 Function

The Meantimer finds the mean time of two PMT signals. The two PMTs are connected to a single piece of scintillator, thus forming one detector. A particle striking the scintillator will generally be closer to one PMT or the other. So for any given event one PMT will fire earlier than its partner. This means the individual PMT signals will vary in time considerably from event to event. However, the mean time of the PMTs in one detector will be constant. This is just due to the fixed length of the scintillator.

$$\frac{t_1 + t_2}{2} = \frac{d_1 + d_2}{2c} = \frac{d}{2c} = k \quad (3.1)$$

Here  $t_1$  and  $t_2$  refer to the time of each PMT. The distance of the particle from PMT 1 is  $d_1$ , the distance from PMT 2 is  $d_2$  and the length of the scintillator is  $d = d_1 + d_2$ .

The meantimer principle is fairly simple. Discriminator outputs from the two PMT signals input to separate delay lines. Each delay line is comprised of individual gates, in this case inverters. The internal delay of the individual inverters then determines the minimum resolution of the meantimer. The input signals propagate along the delay lines in opposite directions. A coincidence is formed between pairs of inverters, one from each delay line. The meantime then is simply the time at which the two input signals overlap along the two delay lines. This is shown schematically in figure 3.1.

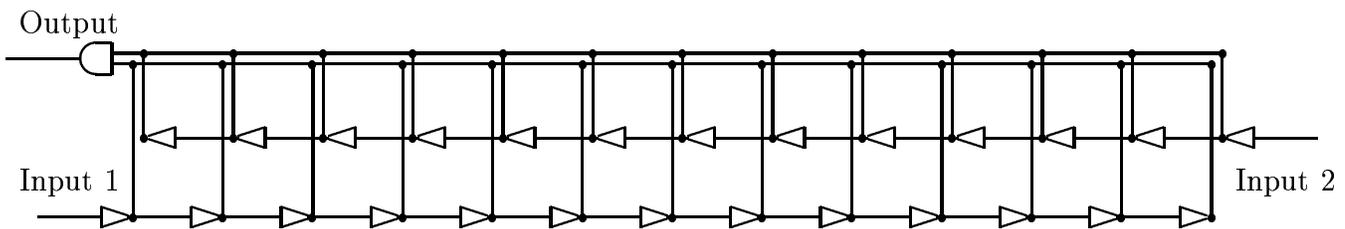


Figure 3.1: The basic principle of a meantimer. Two signals enter two individual delay lines and propagate in opposite directions. The overlap coincidence of the two signals is then the meantime. The delay lines are comprised of inverters. The propagation time of the individual inverters gives the minimum resolution of the meantimer.

An Application Specific Integrated Circuit (ASIC) meantimer has been developed for the G<sup>0</sup> experiment by ISN Grenoble. This ASIC has two meantimer channels in a 28 pin PLCC package. The inverters in the delay lines have been modified from a typical inverter to make what is referred to as a starved inverter. Basically, in the starved inverter the rising and falling edge delays are controlled by an external voltage. This allows for control of the intrinsic delay of the inverters and thus of the meantimer delay lines. Normally the intrinsic delay of an inverter is dependent on the temperature. With the starved inverter, the external voltage may be varied to compensate for intrinsic delay changes due to changes in temperature.

## 3.2 Temperature Compensation

There are two basic methods for temperature compensation with the Grenoble meantimer ASIC. In the first method, each ASIC contains a Voltage Controlled Oscillator (VCO) which is made from the same starved inverters used in the delay lines. So the frequency of the VCO will change in relation to temperature in the same way as the delay lines. Cancelling the temperature drift of the delay lines can then be accomplished by a feed back circuit that compares the frequency of the VCO to that of an external clock.

The second method is to use an external temperature compensation circuit like the one shown in figure 3.2. The LM335 is a temperature sensor which outputs a voltage which is linearly proportional to temperature with a slope of  $10 \text{ mV}/^\circ\text{C}$ . The plus (+) side of the op amp is held at a fixed voltage offset which is set with the  $10\text{k}\Omega$  potentiometer. The minus (-) side is connected to both the output of the temperature sensor and a feedback circuit from the output of the op amp. The op amp adjusts its output voltage such that the plus and minus inputs are equal. Thus the output of the op amp will change in proportion to the temperature. Note that the op amp has the effect of reversing the temperature relation. As the temperature goes up, the output of the LM335 goes up and the output of the op amp must go down to compensate. Likewise, if the temperature goes down, the output of the op amp will go up.

For the temperature compensation to work properly, the voltage on the plus (+) side of the op amp has to be set to the correct level. It is important to pick a control voltage offset so that slope of the delay versus temperature is zero. As can be seen in figure 3.5 a voltage of  $-1.33\text{V}$  on the plus side of the will result in a nearly constant delay over a wide range of temperatures.

The potentiometer in the external compensation circuit (figure 3.2) is used to set the nominal control voltage of the ASIC. Basically, the op amp will hold the control pin at this voltage at a given temperature. The temperature sensor will then cause the op amp to change this voltage by  $10 \text{ mV}/^\circ\text{C}$  as the ambient temperature changes. The procedure for setting the pot is as follows. Turn on the meantimer and allow the module to warm up. The ambient temperature in the room should be between  $20$  and  $30 \text{ }^\circ\text{C}$ . At this temperature, set the pot so the voltage on the plus side of the op amp is  $-1.33\text{V}$ .

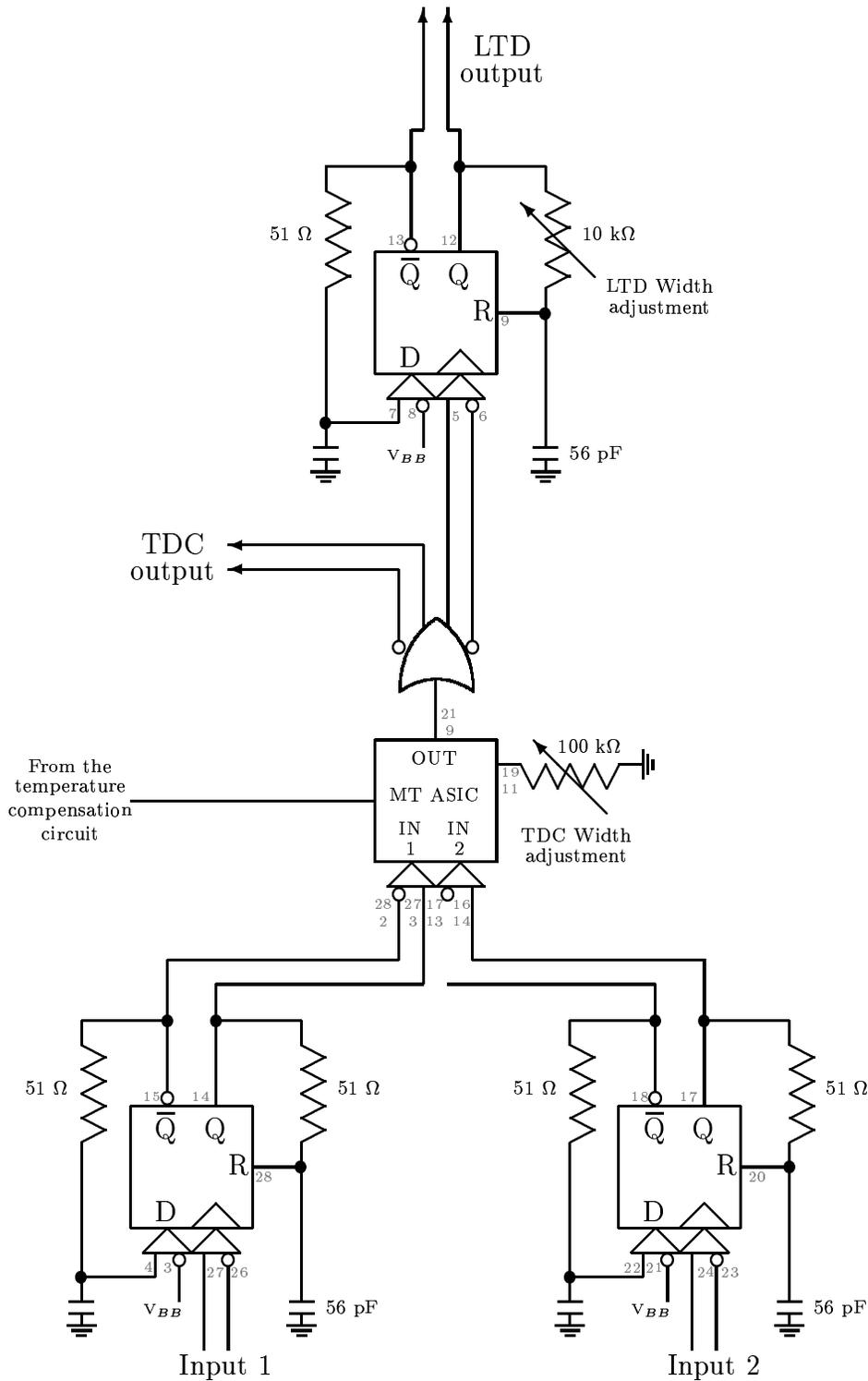


Figure 3.2: The schematic for a single meantimer channel. Inputs 1 and 2 refer to signals from the two PMTs at each end of a scintillator. These signals come from the CFD. The RC circuits on the reset of the latches are designed to keep the widths of the pulses short, to prevent accidental overlaps within the meantimer. The MT ASIC has a monostable adjustment which sets the width of the TDC output and the deadtime of the channel. The RC circuit on the reset of the output latch sets the width of the pulses going to the LTD.

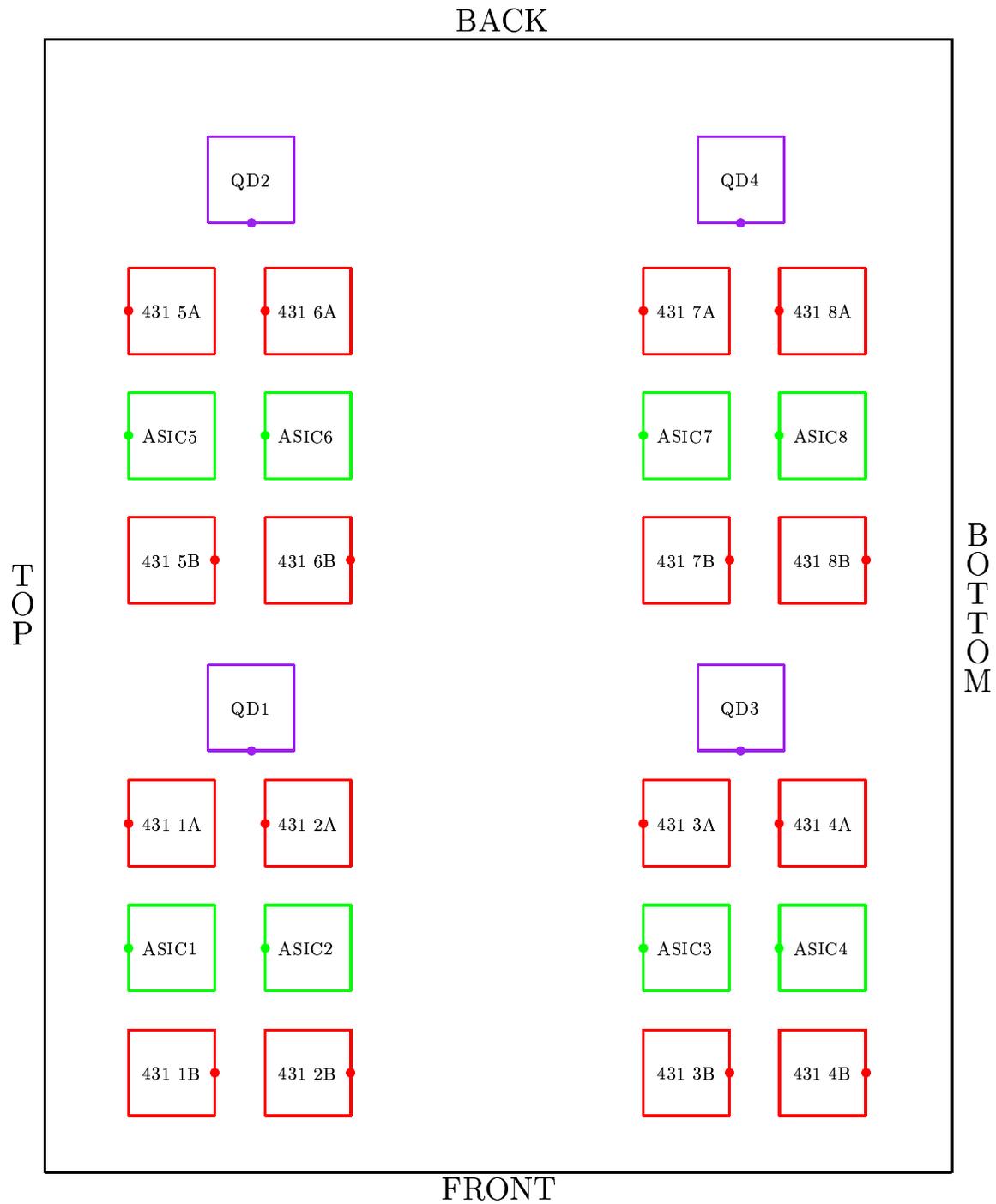


Figure 3.3: Chip positions for the meantimer board. See table 6.3 for the meaning of the labels. The dots show the position of pin 1. See table D.1 for the pin arrangement of the PLCC chips.

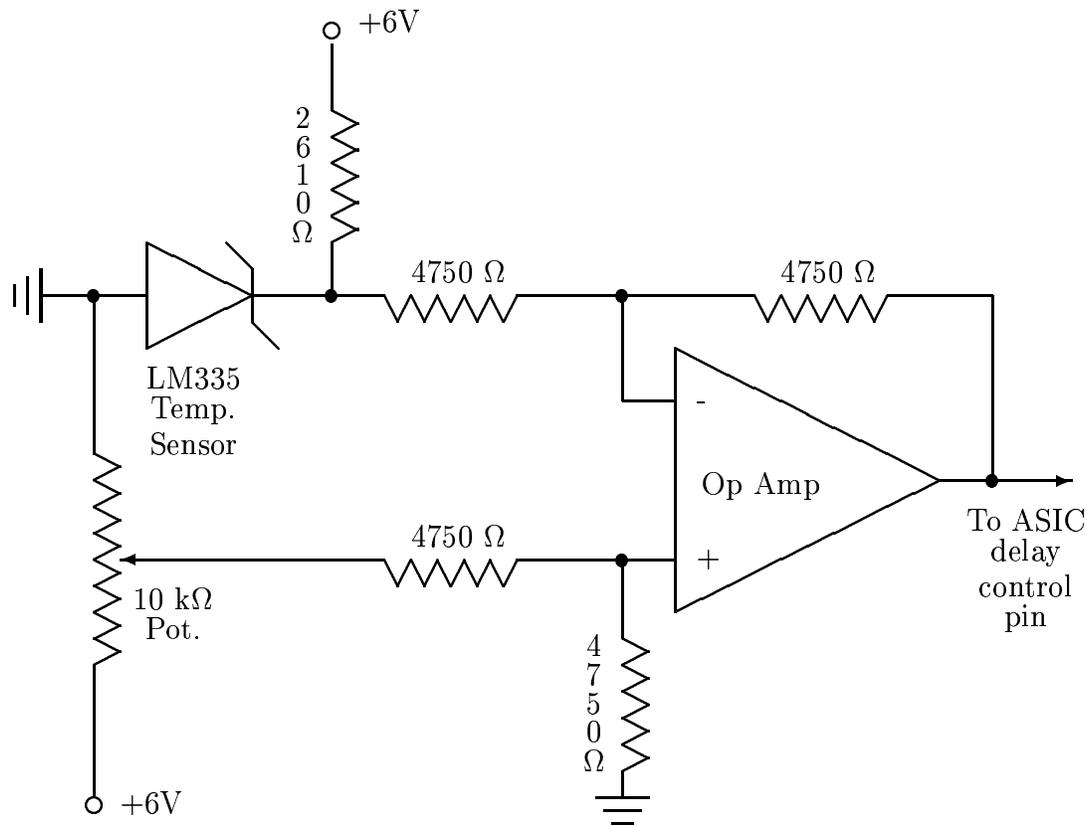


Figure 3.4: The external temperature compensation circuit for the Grenoble meantimer ASIC.

### 3.3 Inputs and Outputs

The front panel for the North American meantimer NIM module is shown in figure 3.3. There are two 34 pin male ribbon connectors labelled IN 1 and IN 2 for the 32 input signals of the 16 meantimer channels. Each meantimer channel produces two outputs, one for a TDC and one for a LTD. The TDC outputs go through the 34 pin male ribbon connector labelled TDC OUTPUT. There are 4, 10 pin male ribbon connectors for the LTD outputs. These are labelled LTD1, LTD2, LTD3 and LTD4. Table 3.3 shows how the pins on the input connectors map to the TDC and LTD output connectors. Table 3.3 shows how the front and backup PMTs should be connected to the meantimer inputs. On the back of the meantimer NIM module there is a standard NIM power connector with pin assignments listed in table 3.3. Only pins 10,11,33,41 and 42 are used for this module.

### 3.4 Internal Settings

There are three basic internal settings for each meantimer channel. These are the LTD output width, the TDC output width and the temperature compensation offset (see section 3.2). The LTD and TDC output widths are adjusted using potentiometers on the meantimer printed circuit board. They are accessible by opening the meantimer NIM module on the right hand side (as viewed from the front). These pots are labelled yellow for LTD widths and blue for TDC widths and red for the temperature compensation offsets. The channel assignments listed in table 3.4. The LTD widths have a range of 0 to 20 ns, the TDC widths have a range of 0 to 2  $\mu$ s. Each temperature compen-

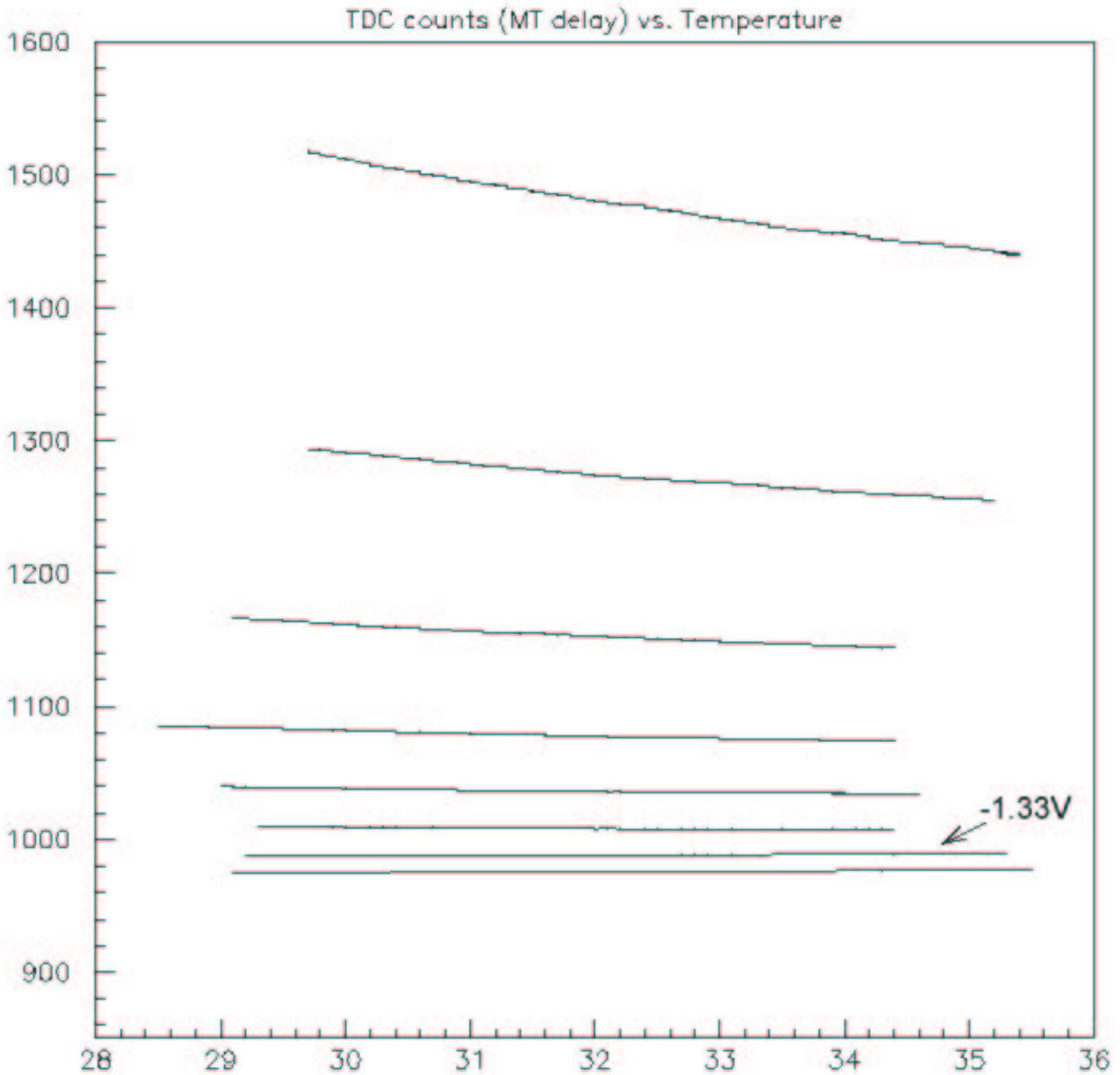


Figure 3.5: Meantimer propagation delay versus temperature taken for various settings of the control voltage. When the plus (+) side of the op amp is set to  $-1.33\text{V}$ , the slope of the curve is at its minimum.

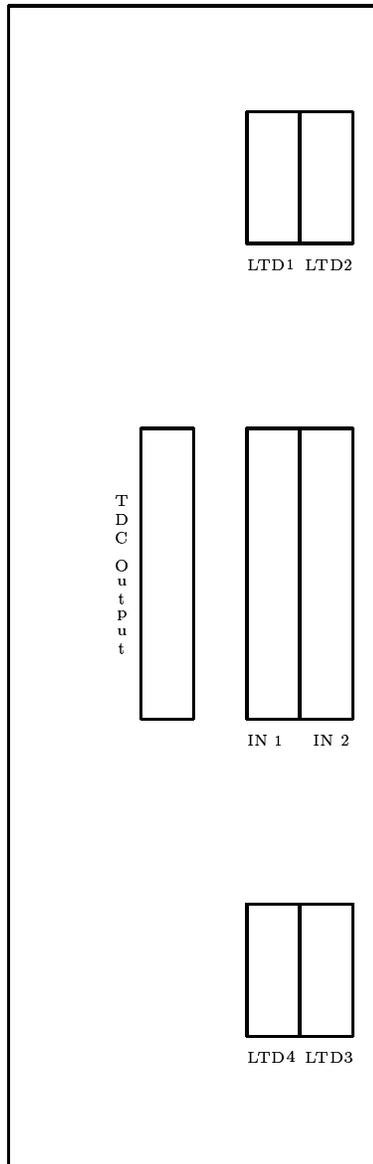


Figure 3.6: The front panel for the North American meantimer NIM module.

Input Con.	Ch.	PMT 1 Pins	PMT 2 Pins	TDC Pins	LTD Con.	Pins
1	1A	1, 2	5, 6	1, 2	1	1, 2
1	2A	3, 4	7, 8	3, 4	2	1, 2
1	1B	9,10	13,14	5, 6	1	7, 8
1	2B	11,12	15,16	7, 8	2	7, 8
1	3A	17,18	21,22	17,18	3	1, 2
1	4A	19,20	23,24	19,20	4	1, 2
1	3B	25,26	29,30	21,22	3	7, 8
1	4B	27,28	31,32	23,24	4	7, 8
2	5A	1, 2	5, 6	9,10	1	3, 4
2	6A	3, 4	7, 8	11,12	2	3, 4
2	5B	9,10	13,14	13,14	1	9,10
2	6B	11,12	15,16	15,16	2	9,10
2	7A	17,18	21,22	25,26	3	3, 4
2	8A	19,20	23,24	27,28	4	3, 4
2	7B	25,26	29,30	29,30	3	9,10
2	8B	27,28	31,32	31,32	4	9,10

Table 3.1: Map of the meantimer inputs and outputs.

Pins	Input 1	Input 2
1, 2	LTD 1, backup 1, PMT 1	LTD 1, backup 2, PMT 1
3, 4	LTD 2, backup 1, PMT 1	LTD 2, backup 2, PMT 1
5, 6	LTD 1, backup 1, PMT 2	LTD 1, backup 2, PMT 2
7, 8	LTD 2, backup 1, PMT 2	LTD 2, backup 2, PMT 2
9,10	LTD 1, front 1, PMT 1	LTD 1, front 2, PMT 1
11,12	LTD 2, front 1, PMT 1	LTD 2, front 2, PMT 1
13,14	LTD 1, front 1, PMT 2	LTD 1, front 2, PMT 2
15,16	LTD 2, front 1, PMT 2	LTD 2, front 2, PMT 2
17,18	LTD 3, backup 1, PMT 1	LTD 2, backup 2, PMT 1
19,20	LTD 4, backup 1, PMT 1	LTD 2, backup 2, PMT 1
21,22	LTD 3, backup 1, PMT 2	LTD 2, backup 2, PMT 2
23,24	LTD 4, backup 1, PMT 2	LTD 2, backup 2, PMT 2
25,26	LTD 3, front 1, PMT 1	LTD 2, front 2, PMT 1
27,28	LTD 4, front 1, PMT 1	LTD 2, front 2, PMT 1
29,30	LTD 3, front 1, PMT 2	LTD 2, front 2, PMT 2
31,32	LTD 4, front 1, PMT 2	LTD 2, front 2, PMT 2

Table 3.2: Map of the PMT input connections for the meantimer.

Pin	Function	Pin	Function
1	+3 VDC	22	reserved
2	3 VDC	23	reserved
3	spare bus	24	reserved
4	reserved bus	25	reserved
5	coaxial	26	spare
6	coaxial	27	spare
7	coaxial	28	+24 VDC
8	200 VDC	29	24 VDC
9	spare	30	spare bus
10	+6 VDC	31	spare
11	6 VDC	32	spare
12	reserved bus	33	117 VAC (hot)
13	spare	34	power return gnd
14	spare	35	reset (scaler)
15	reserved	36	gate
16	+12 VDC	37	reset (aux)
17	12 VDC	38	coaxial
18	spare bus	39	coaxial
19	reserved bus	40	coaxial
20	spare	41	117 (neut)
21	spare	42	high quality gnd

Table 3.3: NIM power connector.

Channel	LTD	Detector	LTD Width (yellow)	TDC Width (blue)	Temp. Comp. (red)
1A	1 top	backup	L1S1	T01	TC1
2A	1 top	front	L1B1	T02	TC1
1B	2 top	backup	L2S1	T03	TC1
2B	2 top	front	L2B1	T04	TC1
3A	3 top	backup	L3S1	T09	TC2
4A	3 top	front	L3B1	T10	TC2
3B	4 top	backup	L4S1	T11	TC2
4B	4 top	front	L4B1	T12	TC2
5A	1 bottom	backup	L1S2	T05	TC3
6A	1 bottom	front	L1B2	T06	TC3
5B	2 bottom	backup	L2S2	T07	TC3
6B	2 bottom	front	L2B2	T08	TC3
7A	3 bottom	backup	L3S2	T13	TC4
8A	3 bottom	front	L3B2	T14	TC4
7B	4 bottom	backup	L4S2	T15	TC4
8B	4 bottom	front	L4B2	T16	TC4

Table 3.4: List of potentiometers for setting widths in the Meantimer module.

station pot controls the voltage offset for 2 meantimer ASICs, each of which has two channels.

### 3.5 Module Construction

Figure 3.7 shows the layout of the meantimer six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the meantimer module is given in table 3.5.

Figure 3.7: Layout of the Meantimer board (MEANTIME.BD1).

Quan.	Description	Manufacturer	Part Number
1	NIM Double wide module	PMF	01-010R
1	NIM power connector male	PMF	202515-1
1	NIM power connector hood	PMF	202394-2
90	0.1 $\mu\text{F}$ ceramic capacitor	Panasonic	ECU-S1H104KBB
48	56 pF ceramic capacitor	Panasonic	ECC-F1H560JC
8	470 $\mu\text{F}$ electrolytic capacitor	Panasonic	ECE-A1AU471
4	1.0 $\mu\text{F}$ tantalum capacitor	Panasonic	ECS-F1VE105K
80	51.1 $\Omega$ resistor	Yageo	MFR-25FBB-51R1
2	88.7 $\Omega$ resistor	Yageo	MFR-25FBB-88R7
32	110 $\Omega$ resistor	Yageo	MFR-25FBB-110R
6	150 $\Omega$ resistor	Yageo	MFR-25FBB-150R
4	2610 $\Omega$ resistor	Yageo	MFR-25FBB-2K61
16	4750 $\Omega$ resistor	Yageo	MFR-25FBB-4K75
40	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
4	8 pin 51 $\Omega$ resistor network	CTS corp.	77081510
16	3-Bit Diff. Flip-Flop	On Semiconductor	MC100E431FN
4	Quad Driver	Micrel	SY100E112JC
8	Grenoble MT ASIC	ISN Grenoble	
28	28 pin PLCC socket	FCI	PLCC-28-P-T
16	1.0 K $\Omega$ Potentiometer	Bourns	3296W-1-102
4	10 K $\Omega$ Potentiometer	Bourns	3296W-1-103
16	100 K $\Omega$ Potentiometer	Bourns	3296W-1-104
4	Temperature sensor	National Semiconductor	LM335AZ
1	AC/DC PCB power supply	Cosel U.S.A.	YS1505A
3	Negative Voltage Reg.	National Semiconductor	LM337T
1	Positive Voltage Reg.	National Semiconductor	LM317T
4	Operational Amplifier	Texas Instr.	OP07CP
4	8 pin DIP socket	Mill-Max	110-93-308-41-001
4	10 pin PCB DIN con.	3M	2510-6002UB
4	10 Pin DIN con. w/flanges	3M	4610-6050
3	34 pin PCB DIN con.	3M	2534-6002UB
3	34 Pin DIN con. w/flanges	3M	4634-6000

Table 3.5: Parts List for Meantimer

# Chapter 4

## Clock Gating Board (KGB)

### 4.1 Function

### 4.2 Inputs and Outputs

Tables 4.2 and 4.2 show the inputs and outputs for the KGB. These will be explained below. Figure 4.2 shows the nominal setup for the clock crate. The YO signal is the beam pickoff synchronization signal. This and the 500 MHz clock (phase shifted to be synchronized with the YO) are provided by CEBAF. These two signals are input to the KGB through twinaxial cables.

A third input to the KGB is the CLK DISABLE. This input can be either differential ECL with a twinaxial connector, or NIM with a standard Lemo connector. The DISABLE jumper on the KGB must be set to either ECL (pins 1 and 2) or NIM (pins 2 and 3) depending on the choice of input for the CLK DISABLE. The purpose of the CLK DISABLE is to turn off the clock trains at the end of a macropulse. This way the LTDs will be quiet while the scalers are being read out. An ECL high (-0.9 V) or NIM false (0 V) on this input will disable the clock trains. An ECL low (-1.7 V) or NIM true (-0.9 V) on this input will enable the clock trains. The CLK DISABLE is synchronized to the YO so that it won't disable the clock trains till the first YO after the disable is turned on (ECL high or NIM false). In this way, there will always be a complete clock train no matter when the CLK DISABLE is initiated. Likewise, the first YO after the disable is turned off (ECL low, NIM true) will produce a complete clock train.

The outputs of the KGB are one copy of the *SYNC* pulse, plus eight copies of the gated clock train (*CLK 0* to *CLK 7*). The SDB has two inputs, *CLK* and *SYNC*. The outputs are eight copies of each of these (*CLK 0* to *CLK 7* and *SYNC 0* to *SYNC 7*).

To make enough copies of the *SYNC* and *CLK* for all the LTD boards, 5 of the *CLK* outputs from the KGB each go to a SDB. Each of these SDBs make 8 copies, for a total of 40 outputs. Since the KGB only makes one copy of the *SYNC* pulse, a SDB is used to produce the 5 copies needed for the SDBs which feed the LTDs. Figure 4.2 shows how these are connected. A single SDB has a propagation delay of 3 ns. The *CLK* signals go from the KGB, through 16 ns cables to a SDB, then through 16 ns cables to the LTDs. The total path length is then 35 ns. The *SYNC* signal goes from the KGB to the first SDB through a 13ns cable. From this SDB it goes to a second SDB through 8 ns cables, then through 8 ns cables to the LTDs. The cable lengths were chosen so the delay of *SYNC* would be the same as the delay of the *CLK*, 35 ns.

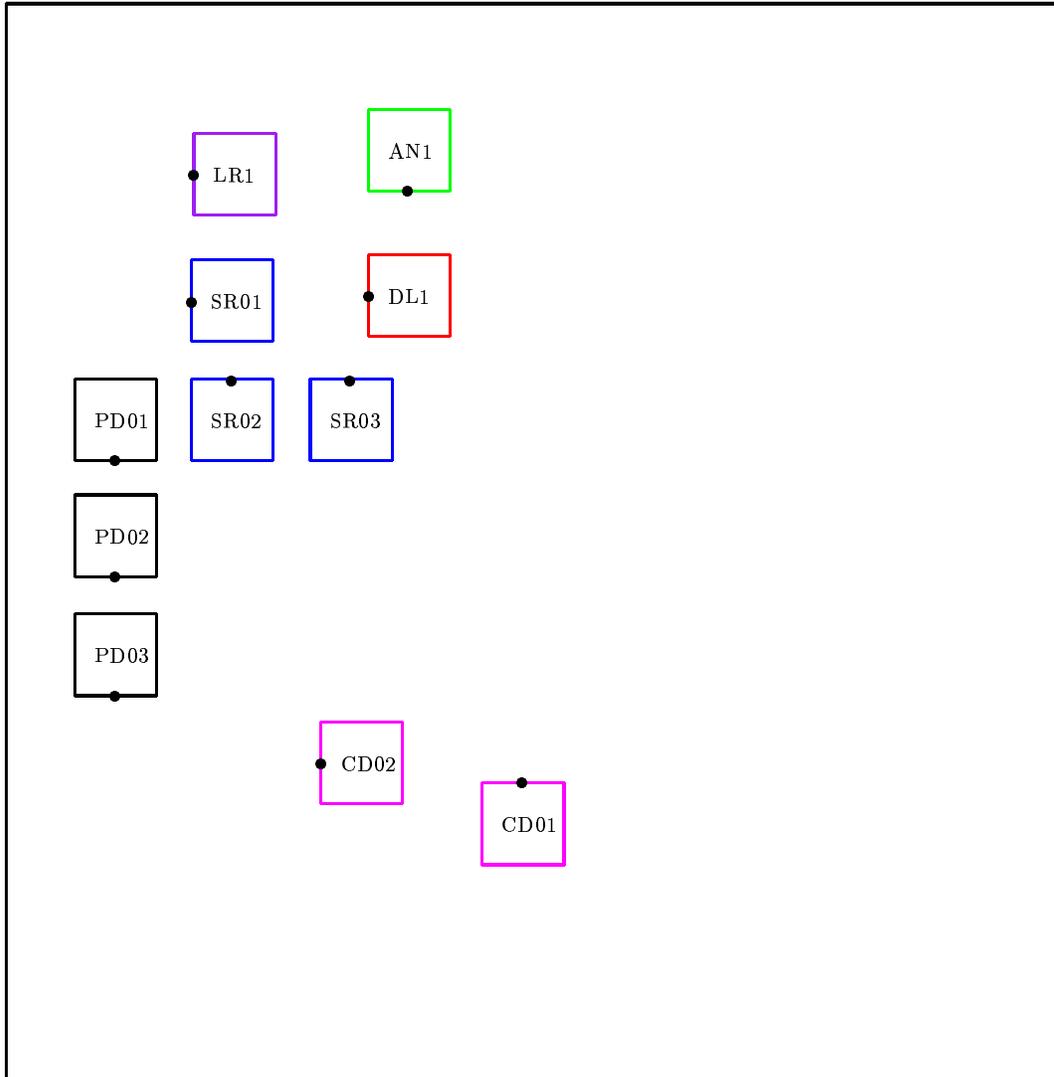


Figure 4.1: Chip positions for the KGB board. See table 6.3 for the meaning of the labels. The dots show the position of pin 1. See table D.1 for the pin arrangement of the PLCC chips.

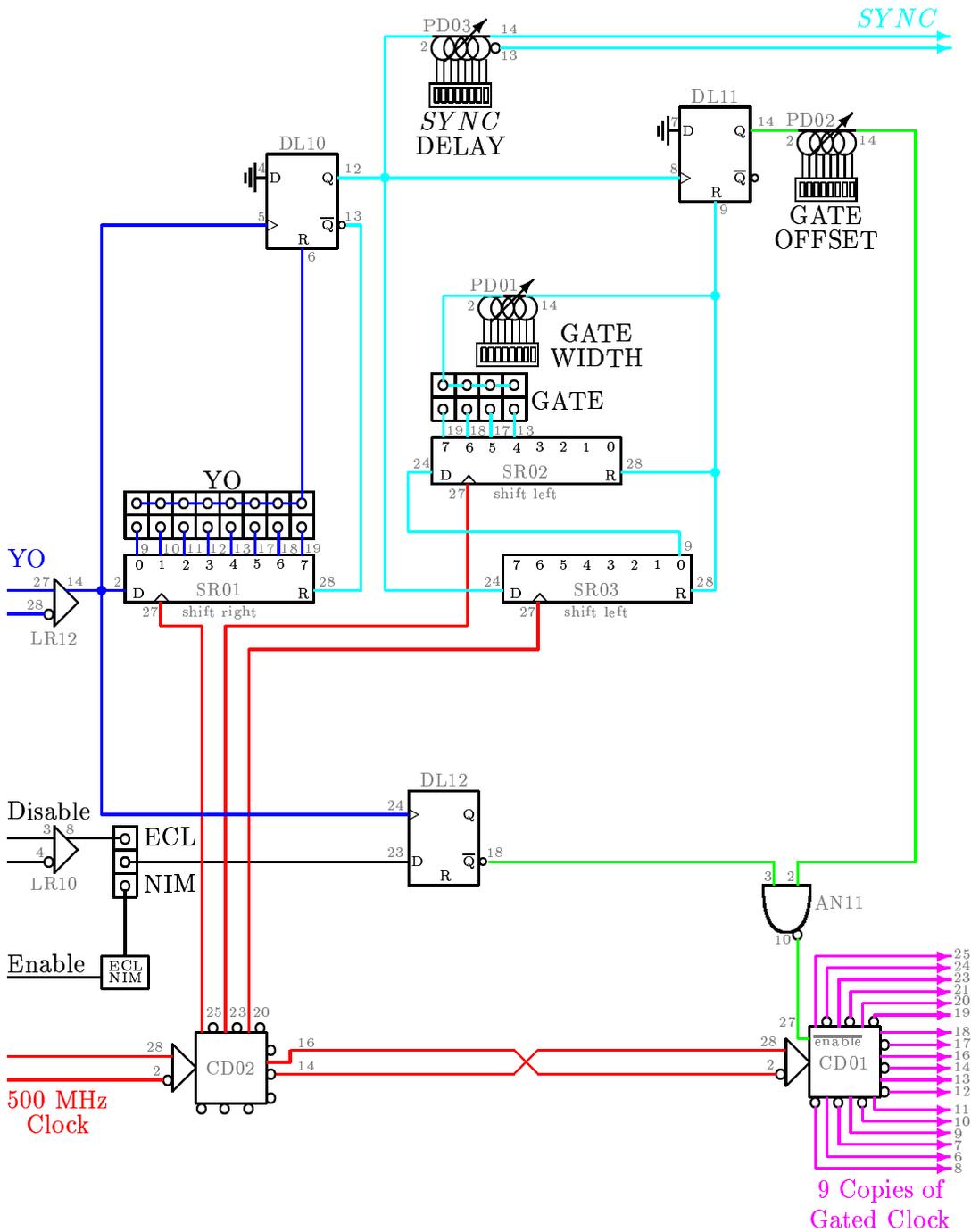


Figure 4.2: Block diagram for the KGB. The 500 MHz clock input lines are in red. The gated clock train outputs are magenta. The YO input lines are blue and the output SYNC lines are cyan. The gate lines are green.

Input	Connector	pins
CLOCK	CLOCK	twinaxial
YO	YO	twinaxial
CLK DISABLE ECL	CLK DISABLE ECL	twinaxial
CLK DISABLE NIM	CLK DISABLE NIM	Lemo coaxial
power GND	POWER HEADER	2,4,6,8,10,12,14,16,18,20
power -5V	POWER HEADER	1,3,5,7,9
power -2V	POWER HEADER	11,13,15,17,19

Table 4.1: Inputs for the KGB.

Input	Connector	pins
SYNC	SYNC	twinaxial
CLK 0	CLK 0	twinaxial
CLK 1	CLK 1	twinaxial
CLK 2	CLK 2	twinaxial
CLK 3	CLK 3	twinaxial
CLK 4	CLK 4	twinaxial
CLK 5	CLK 5	twinaxial
CLK 6	CLK 6	twinaxial
CLK 7	CLK 7	twinaxial

Table 4.2: Outputs for the KGB.

The front panel of the KGB is shown in figure 4.5. There are three Lemo twinaxial connectors, one for the 500 MHz clock, one for the YO signal and one for the KGB disable. There is also a Lemo coaxial connector for the KGB disable. The twinaxial connector is for differential ECL input of the disable signal and the coaxial connector is for NIM input of the signal. The DISABLE jumper on the board decides which of these two inputs is used. The power header plugs into the power connections on the back plane of the clock crate and accepts the -5.2V and -2.0V needed for the board.

On the printed circuit board (see figure 4.8) there are places for a total of 9 twinaxial outputs of the gated clock signal. However, only 5 are actually filled to fan out to the signal duplication boards (SDBs) (see chapter 5). There is an additional twinaxial output connector for the *SYNC* signal.

### 4.3 Internal and External Settings

The KGB has six different internal settings, three jumpers on the board see table 4.3 and three programmable delays accessible from the front panel (see figures 4.8 and 4.5). The DISABLE jumper near the top, front side of the board chooses between ECL or NIM input for the DISABLE signal. Below this is the YO jumper with 8 settings labelled 2 ns to 16 ns. This jumper sets the width of the *SYNC* pulse. The GATE jumper is below the YO jumper and has 4 settings labelled 18 ns to

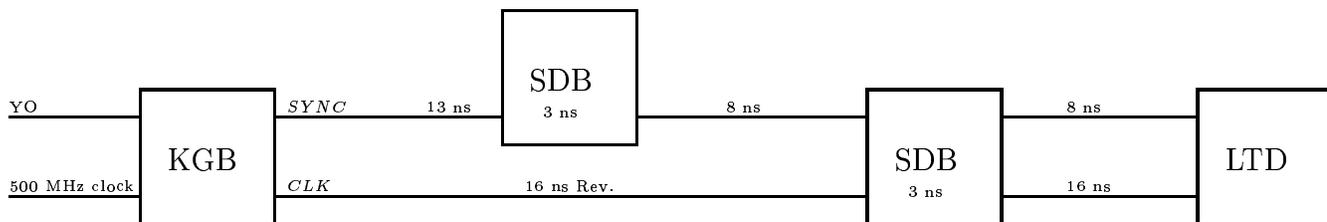


Figure 4.3: The Clock crate connections. This diagram path of a single *SYNC* and clock train signal (*CLK*) from the KGB to the LTD. The internal delay of the SDB is 3ns. So the total delay for the clock path is  $16 + 3 + 16 = 35$  ns and the total delay for the *SYNC* path is  $13 + 3 + 8 + 3 + 8 = 35$  ns. The first SDB in the *SYNC* path takes one copy of *SYNC* from the KGB and makes 5 copies. The SDB in the *CLK* path is one of 5 modules. Each takes one copy of the *SYNC* and *CLK* signals and makes 8 copies.

Name	Function
DISABLE	Sets CLK DISABLE input to accept NIM or ECL
YO	Sets the width of the <i>SYNC</i> pulse
GATE	Sets the width of the gate within 2 ns for the clock train

Table 4.3: List of jumpers on the KGB.

24 ns. This jumper sets the width of the gate in 2 ns increments. It is used in conjunction with the GATE WIDTH programmable delay.

On the front of the KGB are three sets of 8 DIP switches. These control three different programmable delay chips (Micrel, SY100E195). On each, the top switch is not used, the second switch from the top is the most significant bit and the bottom switch is the least significant bit. Setting the bottom switch will give the minimum delay of the chip which is roughly 20 ps. Setting the second switch from the bottom will give 40 ps of delay, the third 80 ps, and so forth. Each switch is double the delay of the switch below it. Figure 4.3 shows the preferred, nominal settings of the KGB. The figure shows the ungated 500 MHz clock, the disable gate generated by the KGB, the resulting clock train and SYNC pulse. Note that the edges of the gate each fall between two clock pulses. The gate width, gate offset and *SYNC* delay are all controlled by programmable delays which are set by the three DIP switches on the front panel. The function of these delays will be described below.

The first set of DIP switches are labelled GATE WIDTH. The GATE jumper on the board sets the width of the gate in 2 ns increments. The GATE WIDTH programmable delay adds additional delay to this. How this effects the gated clock train is shown in figure 4.3. Increasing or decreasing the width of the gate will add or subtract pulses from the clock train. The figure also shows that because of the fine resolution of the programmable delay, it is possible change the width of the gate so that it falls during a clock pulse. In this case, that particular pulse will be truncated by the gate in the clock train, resulting in a short pulse which is often called a glitch. Both edges of each clock pulse in the train are used by the LTD boards for time digitization. Since the edges of a glitch are closer together than the nominal 1 ns, they will result in a narrow time bin. Therefore glitches should be avoided when setting the KGB parameters. The glitch in figure 4.3 would be counted as

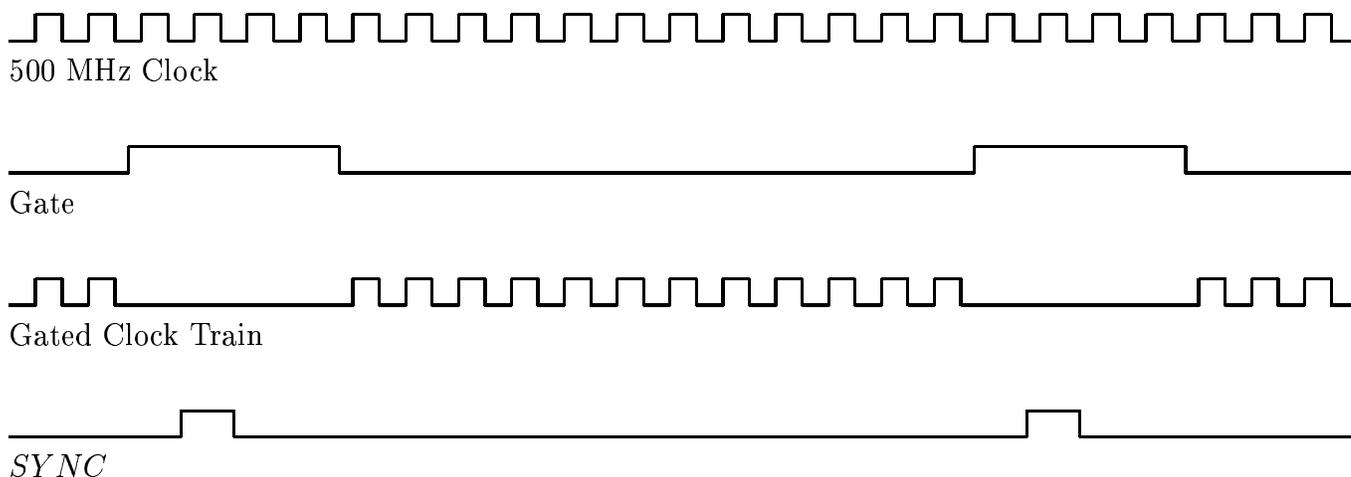


Figure 4.4: The nominal KGB settings should produce a clock train with 12 pulses followed by an 8 ns gate. In this diagram, the gate (clock disable) is 24 ns wide with 8 ns between gates. The edges of the gate are centered between clock pulses. This produces the clock train required by the LTDs. The *SYNC* pulse is produced from the beam YO pulse.

a 13th pulse, so the error lights on the LTD front panels would register “TOO MANY.”

The second set of DIP switches are labelled GATE OFFSET. This programmable delay adds delay to the GATE relative to the 500 MHz clock. The purpose is to shift the gate so that both the rising and falling edge fall between clock pulses. This ensures there will be no glitches in the clock train. Figure 4.3 shows the effect of shifting the gate by 1 ns relative to a nominal gate. In this case, both edges fall during a clock pulse, so each pulse is truncated producing glitches. Again, the clock train in figure 4.3 has 13 pulses (11 good pulses plus 2 glitches) so the error lights on the LTD front panels would indicate “TOO MANY.”

The third set of DIP switches are labelled SYNC DELAY. This programmable delay adds delay to the *SYNC* pulse which is produced from the beam YO pulse. The *SYNC* pulse is used by the LTD boards to check the integrity of clock train. It also resets the shift registers on the LTDs that produce the signals to strobe and clear the input latches, shift registers and D registers. Changes to the *SYNC* delay do not effect the gated clock train itself. However, if the *SYNC* comes during the clock train, the LTDs will count the wrong number of clock pulses and produce the clear and stobe signals at the wrong times. It will also result in the LTD error lights registering “TOO FEW.” The effect of the SYNC DELAY are shown in figure 4.3.

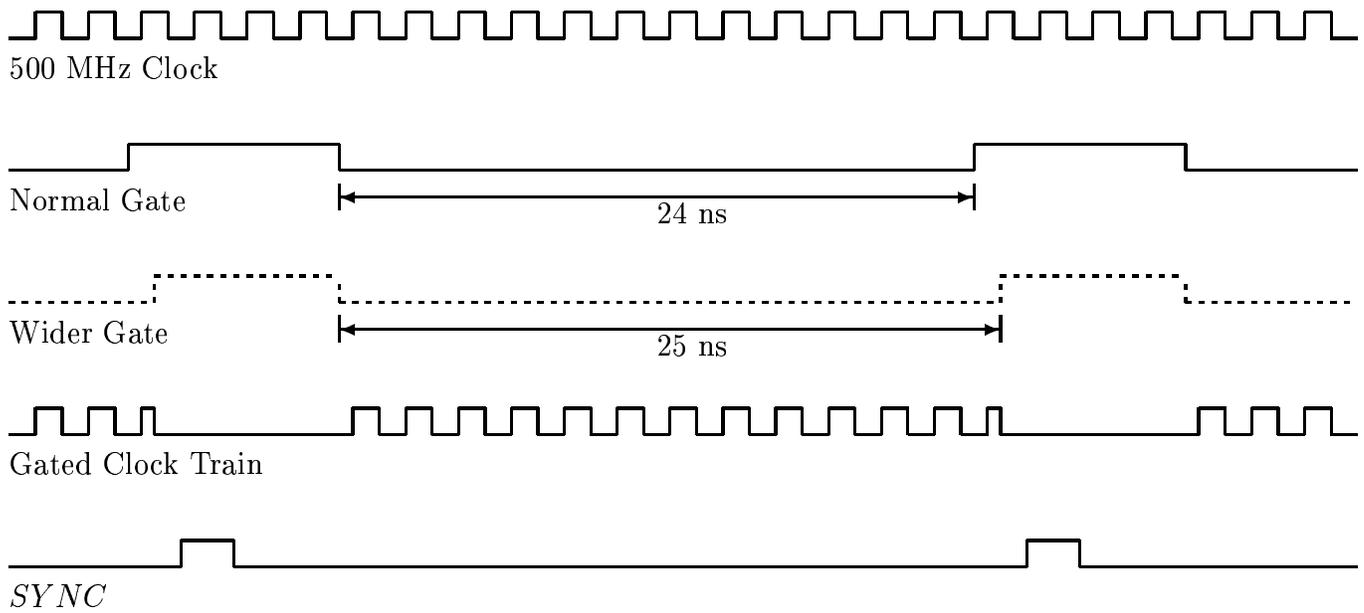


Figure 4.5: The effect of the GATE WIDTH switches is to increase or decrease the length of the gate. In this diagram, the gate width has been increased from 24 ns to 25 ns. The effect of this wider gate is to increase the number of pulses in the clock train and to decrease the size of the gated off portion. The extra clock pulse is a glitch because the gate closes in the middle of the pulse. The *SYNC* pulse is unaffected.

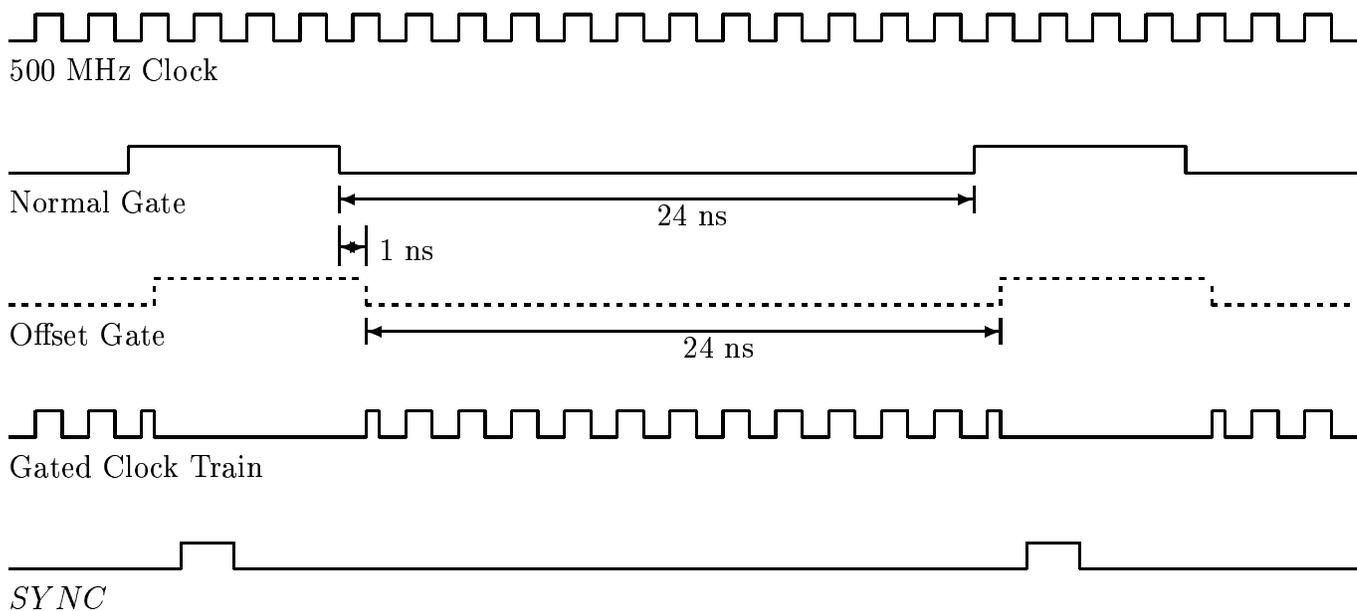


Figure 4.6: The GATE OFFSET switches shift the position of the gate relative to the 500 MHz clock. Generally this is used to center the edges of the gate between clock pulses. In the diagram above, the gate has been shifted by 1 ns (dashed line) so that the edges now fall in the middle of two clock pulses. The result is a clock train with 13 pulses, two of which are glitches. The *SYNC* pulse is unaffected

## 4.4 How to Get the Perfect Clock Train

The best way to obtain the perfect clock train is to start by viewing it with an oscilloscope at the LTD. There are three ways to view the clock train. First, there are differential ECL outputs on the front panel of the LTDs. These can be easily reached with a scope probe. Second, you can place a probe on pin 27 of any shift register (see figure 6.17). The easiest shift registers to access are numbers 9 and 10 in the upper left hand corner of the LTD board. Pin 27 will be the third pin from the left of the bottom row on the chip holder (see figure D.1). Lastly, you can use the G0 twinax to lemo converter box to view both sides of the clock (*CLK* and  $\overline{CLK}$ ). The current adapter box at Jefferson Lab requires a scope with 50  $\Omega$  input impedance and the signals are attenuated by a factor of 10. An alternative to viewing the clock train with an oscilloscope is to watch the error lights on the LTDs. These lights will indicate if there are too many (more than 12) or too few (less than 12) clock pulses. They will also indicate if there is no *SYNC* pulse. However, they will not give you information about the quality of the clock train. For instance, the LTDs will count a glitch pulse as a good pulse, but the width of that bin will be smaller than expected. You can check the bin widths by taking data, but this is a time consuming method to set the clock train. It is best to use an oscilloscope.

Figure 4.3 shows an optimal clock train produced by the KGB. There are four parameters that can be set with the KGB, the width and offset of the clock gate and the width and delay of the *SYNC* pulse. To set the number of pulses in the clock train, first choose a setting for the GATE jumper on the KGB (see table 4.3). In most cases, 22 ns is the best setting. Now count the number of clock pulses in the clock train. If there are 12 full pulses (no glitches, each pulse 1 ns

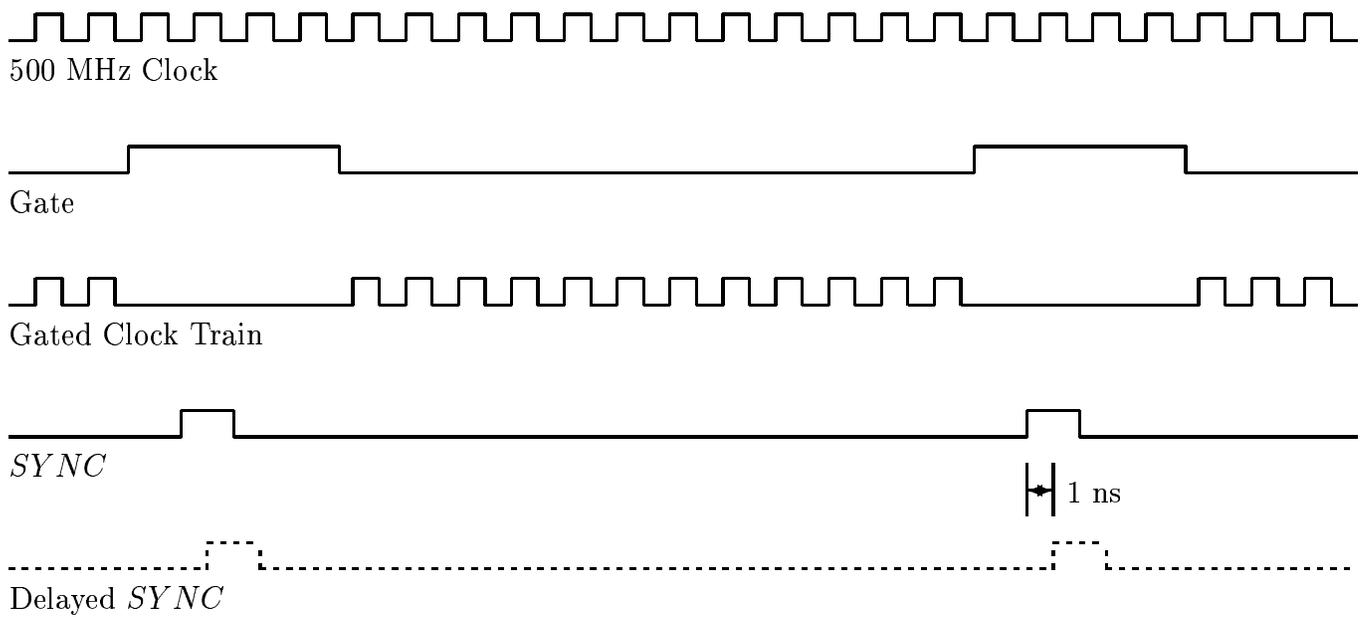


Figure 4.7: The SYNC DELAY switches move the position of the *SYNC* pulse relative to the 500 MHz clock. In this diagram, the *SYNC* pulse has been delay by 1 ns (dashed line). Moving the *SYNC* pulse has no effect on the clock train.

Quan.	Description	Manufacturer	Part Number
21	0.1 $\mu$ F ceramic capacitor	Panasonic	ECK-F1E104ZV
2	470 $\mu$ F electrolytic capacitor	Panasonic	ECE-A1AU471
7	0.01 $\mu$ F ceramic capacitor	KEMET	CK05BX103K
9	51.1 $\Omega$ resistor	Yageo	MFR-25FBF-51R1
3	110 $\Omega$ resistor	Yageo	MFR-25FBF-110R
1	24.9 $\Omega$ resistor	Yageo	MFR-25FBF-24R9
1	511 $\Omega$ resistor	Yageo	MFR-25FBF-511R
11	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
11	28 pin PLCC socket	FCI	PLCC-28-P-T
1	Quad 2-Input AND Gate	Micrel	SY100E104JC
2	1:9 Differential Clock Driver	Micrel	SY100E111JC
1	Quad Differential Line Receiver	Micrel	SY100E116JC
1	4-Bit D Flip-Flop	Micrel	SY100E131JC
3	8-Bit Shift Register	Micrel	SY100E141JC
3	Programmable Delay	Micrel	SY100E195JC
12	twinaxial receptacle	Lemo	EPL.0S.302.HLN
1	coaxial receptacle	Lemo	EPL.00.250.NTN
3	8 position DIP switch	CTS corp.	208-8
1	push button switch red cap	Cutler-Hammer	B8600 P281R
1	20 pin RA socket DIN con.	Hirose	PCN13-20S-2.54DS
12	dual row header	Sullins Electronics	PTC36DAAN
3	single row header	Sullins Electronics	PTC36SAAN
1	NPN bipolar transistor	NTE elec.	NTE108

Table 4.4: Parts List for the KGB.

wide) then you will not need to change the GATE WIDTH or GATE OFFSET. Just make sure the *SYNC* pulse does not overlap the clock train at the LTD. You can view the *SYNC* pulse on pin 28 of shift registers 9 and 10 (upper left hand corner) on the LTD board. If the *SYNC* does overlap the clock train, you will need to reduce the SYNC DELAY (see section 4.3).

## 4.5 Module Construction

Figure 4.8 shows the layout of the KGB six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the KGB module is given in table 4.5.

Figure 4.8: Layout of the KGB board (KGB.BD1).

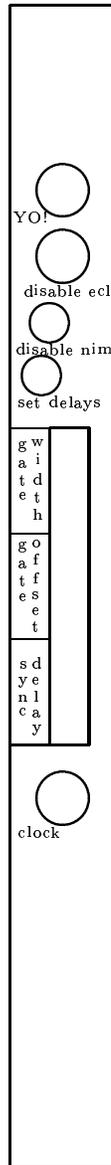


Figure 4.9: The front panel for the Clock Gating Board (KGB).

# Chapter 5

## Signal Duplication Board (SDB)

### 5.1 Function

The signal duplication board (SDB) takes a copy of the SYNC signal and a copy of the gated clock signal (both generated by the clock gating board, chapter 4) and produces multiple outputs of each.

### 5.2 Inputs and Outputs

The SDB has two Lemo twinaxial input connectors on the front panel (see figure 5.3), one for SYNC and one for the gated clock (CLK). There can be up to 9 outputs for each of the two inputs, though only some of these connectors may be in place. The outputs for the CLK signals are on the back of the module and the outputs for the SYNC signals are on the front of the module. There is a power header on the back that plugs into the clock crate backplane and which provides the -5.2V and -2.0V needed by the board. Table 5.1 lists the SDB inputs and table 5.2 lists the outputs.

### 5.3 Module Construction

Figure 5.1 shows the layout of the SDB six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the SDB module is given in table 5.3.

Input	Connector	pins
CLK	CLK	twinaxial
SYNC	SYNC	twinaxial
power GND	POWER HEADER	2,4,6,8,10,12,14,16,18,20
power -5V	POWER HEADER	1,3,5,7,9
power -2V	POWER HEADER	11,13,15,17,19

Table 5.1: Inputs for the SDB.

Input	Connector	pins
CLK 0	CLK 0	twinaxial
CLK 1	CLK 1	twinaxial
CLK 2	CLK 2	twinaxial
CLK 3	CLK 3	twinaxial
CLK 4	CLK 4	twinaxial
CLK 5	CLK 5	twinaxial
CLK 6	CLK 6	twinaxial
CLK 7	CLK 7	twinaxial
SYNC 0	SYNC 0	twinaxial
SYNC 1	SYNC 1	twinaxial
SYNC 2	SYNC 2	twinaxial
SYNC 3	SYNC 3	twinaxial
SYNC 4	SYNC 4	twinaxial
SYNC 5	SYNC 5	twinaxial
SYNC 6	SYNC 6	twinaxial
SYNC 7	SYNC 7	twinaxial

Table 5.2: Outputs for the SDB.

Quan.	Description	Manufacturer	Part Number
4	0.1 $\mu$ F ceramic capacitor	Panasonic	ECK-F1E104ZV
2	470 $\mu$ F electrolytic capacitor	Panasonic	ECE-A1AU471
4	0.01 $\mu$ F ceramic capacitor	KEMET	CK05BX103K
2	110 $\Omega$ resistor	Yageo	MFR-25FBF-110R
6	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
2	28 pin PLCC socket	FCI	PLCC-28-P-T
2	1:9 Differential Clock Driver	Micrel	SY100E111JC
18	twinaxial receptacle	Lemo	EPL.0S.302.HLN
1	20 pin RA socket DIN con.	Hirose	PCN13-20S-2.54DS

Table 5.3: Parts List for the SDB.

Figure 5.1: Layout of the SDB board (SDB.BD1).

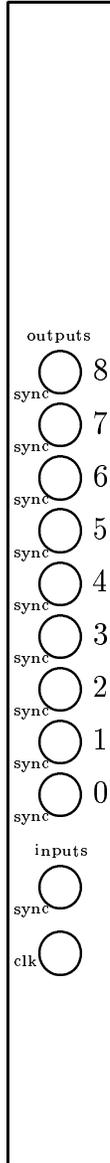


Figure 5.2: The front panel of the SDB.

# Chapter 6

## Latching Time Digitizer Board (LTD)

### 6.1 Function

The purpose of the Latching Time Digitizer (LTD) board is to produce a time of flight (TOF) histogram for the particles of interest in the  $G^0$  experiment (protons in the forward running mode and electrons in the backward running mode). The TOF is measured from the time an electron bunch from the accelerator collides with the target till the time when a particle (proton, electron or inelastics) hits one of the  $Q^2$  detectors. Each LTD board has two input channels. One channel is connected to a single  $Q^2$  detector while the second channel is connected to a detector with the same  $Q^2$  but in the opposite quadrant. The reason for this will be explained in section 6.4. Each LTD channel outputs 24 bits, which are sent to scalars (see chapter 12). These bits represent 24 time bins which cover most of the 32 ns between beam pulses. There are 23 time bins which are 1 ns wide and 1 time bin which is about 6.5 ns in wide. The scalars sum the number of times each bit was set for each detector during a macro pulse to produce the TOF spectra for that detector.

The basic function of the LTD is shown in figure 6.1. This simple diagram is used just for the purpose of instruction. In a very fundamental way, it shows how a single LTD channel works. In truth, the LTD is more complicated than this and so a more detailed explanation will be needed. This will be provided in the sections below.

Each detector in the  $G^0$  experiment is composed of two adjacent scintillators, each of which is viewed by two PMTs, one on each end of the scintillator (see figure 1.1). One scintillator is referred to as the front scintillator and the other is called the back scintillator. The front scintillator is used to set the timing for the TOF measurement while the back scintillator is used as a coincidence detector. On the LTD board, this is accomplished by sending the signal from the back scintillator to the data input of a latch while the signal from the front scintillator is sent to clock input. The back signal will proceed the front signal by a few ns through cable delays and will be about 10 ns in width. At the time the latch sees a rising edge on the clock input it sets the output logic level to the same level as the data input line. So if there is a 1 on the data input, the output will be set and latched to 1 when a signal arrives on the clock line. Likewise, if there is a 0 on the data input, the output will be set and latched to 0 when a signal arrives on the clock line. So the output of the latch will only be set to 1 if there was a hit in both front and back scintillators within a few ns window. Because the front signal is connected to the clock input it determines the timing of the output signal. The input latch is reset, the output goes back to 0, in the second beam pulse after it is set. The reason for this will be discussed in section 6.5.

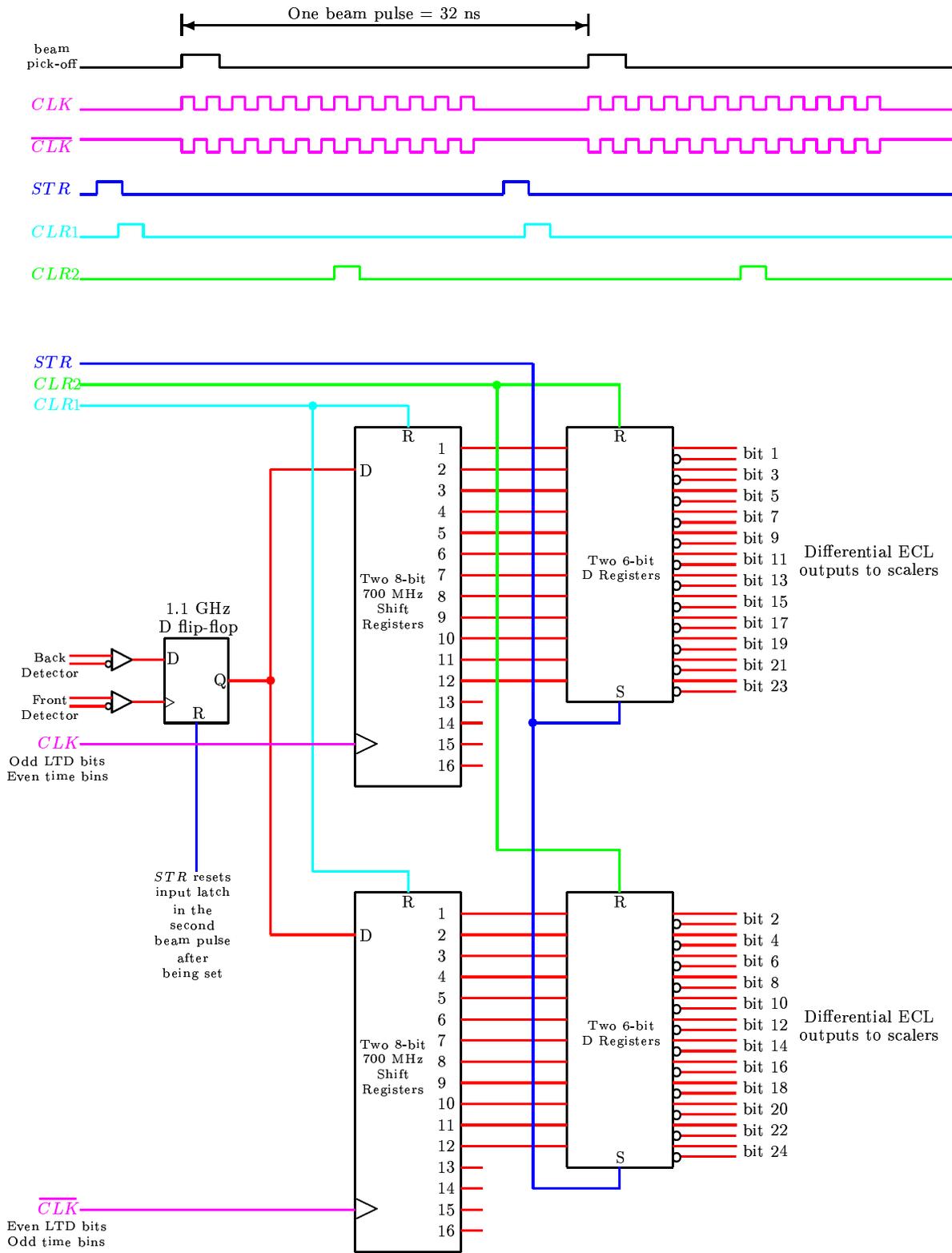


Figure 6.1: The Basic function of the LTD board.

The output of the latch is connected to the input of two 16-bit shift registers (each 16-bit shift register is actually two 8-bit shift registers connected in series). A shift register is similar to a latch but with multiple output bits. When a shift register sees a rising edge on its clock input, it moves the state of the data input into output bit 1. At the same time it moves the previous state of bit 1 into bit 2, the previous state of bit 2 into bit 3 and so forth down the line. In this way, the output bit pattern can be set in serial using successive pulses on the clock input.

In the case of the LTD, the shift register clock pulses are in the form of a 500 MHz gated clock provided by the KGB (see chapter 4). The phase of the clock is matched to the arrival time of the beam pulse on the  $G^0$  target. Gated clock refers to the fact that every 32 ns, the clock is turned off for 8 ns. So there are 12 pulses, each 2 ns apart for a total of 24 ns, followed by a gap of 8 ns as shown in figure 6.1 (*CLK*). This gated clock train of 12 pulses is used to encode the TOF, the time the input latch is set, into the shift register output bits. For instance, imagine that a given detector is hit early in a beam pulse. In this case it will set the input latch before the first clock pulse arrives at the shift register. As a result, the data input of the shift register will be high (1) for all 12 clock pulses and so all 12 output bits will be set to 1 (the last 4 of the 16 bits are not used). If the hit comes halfway through the clock train, say just after the 6th clock pulse, then only the first 6 output bits would be 1, the rest would be 0. So for the first 6 clock pulses, the input latch was not set and there was a 0 on the data input of the shift register, causing 0s to be added to the bit pattern. After the 6th pulse, the input latch was set and there was a 1 on the data input of the shift register, causing a series of 1's to be added to bit pattern. So the number of output bits set to 1 indicates the TOF. The more bits that are set, the earlier the hit came in the beam pulse. Tables 6.1 and 6.1 show this relationship.

One obvious question comes up at this point: Why use an input latch instead of, say, an AND gate for the front and back scintillator coincidence. Once the latch is set in a given beam pulse, it cannot be set again. So if there are multiple hits in a single beam pulse only the earliest is recorded. In addition, using a latch results in the somewhat more complicated relationship between TOF and output bit pattern as shown in table 6.1. If, for instance, the front and back scintillators were connected to an AND gate to form a coincidence, then individual bit numbers would directly correspond to the TOF. Also, multiple hits could be recorded in a single beam pulse. So why not use a simple coincidence for each beam pulse?

In fact, using an input latch removes some ambiguities that would come with using a simple coincidence. First, the overlap of the front and back scintillator signals would result in a variable length pulse. This, in turn, would result in a variable number of shift register bits being set for each hit. Imagine the widths of the two signals are set to be equal ( $w_F = w_B = w$ ) and narrow (a few ns) so that only tight coincidences can be formed. Then the output width of the AND gate would be anywhere from 0 to  $2w$  based on the relative arrival time of the signals. The number of shift register output bits set depends on the width of the coincidence pulse. Therefore the number of bits set would be variable. Since these bits are fed directly into scalars, it would be impossible to tell how often 1 hit fell into multiple time bins. Using the input latch avoids this difficulty since the width of the pulse from the latch is proportional to the arrival time of the front scintillator signal and that arrival time will correspond to just one time bin. The raw time spectrum can be decoded from the scaler data with a simple formula (see equation 6.3) as described below. Second, using an input latch to make the coincidence automatically means the loss of multiple hits in the same beam

TOF (ns)	odd shift register bit pattern	TOF (ns)	even shift register bit pattern
0	111111111111	1	111111111111
2	111111111110	3	111111111110
4	111111111100	5	111111111100
6	111111111000	7	111111111000
8	111111110000	9	111111110000
10	111111100000	11	111111100000
12	111111000000	13	111111000000
14	111110000000	15	111110000000
16	111100000000	17	111100000000
18	111000000000	19	111000000000
20	110000000000	21	110000000000
22	100000000000	23	100000000000
24	000000000000	25	000000000000

Table 6.1: Relationship between the TOF and the output bit pattern of the shift registers. Note that the earlier a hit comes in the beam pulse, the more bits that are set.

pulse. However, again, this is actually an advantage. In general, given the 32 ns spacing of the beam pulses, most of the upstream electronics (such as the CFDs and meantimers) will not recover in a single beam pulse. Therefore, the LTD would not see most of the multiple hits in a single beam pulse anyway. Also, the dead time of the LTD for multiple hits would not be well defined due to the variable width produced by a simple coincidence gate and due to the uncertainties of the upstream electronics (see section 6.3). Therefore, using an input latch gives the LTD a well defined dead time which leads to accurate dead time corrections (see section 6.12).

The clock pulses going to one 16-bit shift register (again, which is actually two 8-bit shift registers coupled together and only 12 bits are used) are spaced 2 ns apart, so the time resolution of this shift register is only 2 ns. The time resolution of the LTD is doubled by using a second 16-bit shift register with an inverted clock train on its clock input. Inverted means the level will be high when the original clock train is low and low when the original clock is high. This is called the clock bar ( $\overline{CLK}$ ) signal. From figure 6.1 it can be seen that the rising edges of  $\overline{CLK}$  coincide with the trailing edges of  $CLK$  and vice versa. So, in essence, the second 16-bit shift register is clocked 180° out of phase with the first 16-bit shift register. This shift register will also have 2 ns resolution, but when combined with the first the total resolution is 1 ns. Therefore the LTD has a total of 24 output bits per channel. The output bits for the first shift register with  $CLK$  are all odd (1,3,5,...), so this is called the odd shift register, while the output bits for the second shift register with  $\overline{CLK}$  are all even (2,4,6,...), so this is called the even shift register.

At the end of a beam pulse, when the 500 MHz clock is gated off for 8 ns, several things happen. First the 12 output bits of the even and odd shift registers are copied in parallel into a set of D registers. A D register is very similar to a latch, it has data, set and reset inputs. A rising edge on the set pin causes the output level to be equal to the level on the data input. A logic high on the reset causes the output to go to 0. Each output bit of both the even and odd shift registers are connected to a single D register. The LTD board uses the gated clock signal to produce several

LTD bit	Time bin	LTD bit	Time bin	LTD bit	Time bin
24	1	16	9	8	17
23	2	15	10	7	18
22	3	14	11	6	19
21	4	13	12	5	20
20	5	12	13	4	21
19	6	11	14	3	22
18	7	10	15	2	23
17	8	9	16	1	24

Table 6.2: Relationship between the LTD bits and the TOF bins. The earliest hit in a beam pulse will set the input latch before the first clock pulse (see figure 6.1) and all the shift register bits will be set when the *STR* pulse comes. Therefore, bit 24 corresponds to the first (earliest) time bin. Likewise, bit 1 corresponds to the last (latest) time bin.

different timing signals (see section 6.7). One of these is the *STR* signal which comes a few ns after the last pulse in the clock train. This signal is connected to all the set pins on the D registers and causes them to read in the shift register output bits, basically storing the output bit pattern. The *STR* is also used to reset the input latch but only in the second beam pulse after it has been set (see section 6.5). The D registers hold the bit pattern for a fixed amount of time (about 16ns) and are reset by the *CLR2* timing signal in the next beam pulse. In this way, the scalers connected to the LTD output bits see pulses with identical widths for every bit that is set. The D register outputs are differential ECL which is required by the scalers. Once the D registers have stored the output bit pattern, the shift registers are cleared with the *CLR1* timing signal. At this point, the LTD is ready for the next beam pulse.

This is the basic function of the LTD. A hit on a detector (with two scintillators) sets an input latch. The time the latch was set is encoded into a bit pattern using a pair of shift registers. The shift registers are clocked at 500 MHz with a gated clock train synchronized to the arrival time of the beam on target. The earlier the latch is set, the more output pits are set on the shift registers. The two shift registers are clocked 180° out of phase to obtain a time resolution of 1 ns. At the end of the beam pulse, the status of the shift register bits are copied to D registers which hold the pattern for a fixed amount of time. After the bits are copied, the shift registers are cleared along with the latch.

The scalers connected to the LTD simply count the number of pulses coming from each LTD output bit. Basically, they count the number of times each bit was set. This sum is read out by computer at the end of each macro pulse (30th of a second) and the scalers are reset. So the scalers accumulate something like a TOF histogram for each detector for each macro pulse. Actually, the scaler data constitutes an integrated TOF histogram. To see this, remember that the number of bits set on the LTD by a hit is related to the time of the hit. If the time bins are labelled as  $j$  (where  $j$  goes from 1 to 24), then the corresponding bit number would be  $i = 25 - j$ . If a hit occurs in time bin  $j$ , then all the bits from 1 to  $25 - j$  will be set. As an example, if a hit comes in time bin 5, then bits 1 to 20 will be set during that beam pulse. Therefore, if  $H_j$  is the number of hits in time bin  $j$ , then the number of times bit  $i$  is set ( $N_i$ ) will be:

$$N_i = \sum_{j=1}^{25-i} H_j \quad (6.1)$$

This shows that the number of counts for each bit is equal to the number of hits in the corresponding time bin plus the sum of all the counts in the lower bits. Equation 6.1 may be used to determine the number of hits in each time bin. Note:

$$\begin{aligned} N_1 &= \sum_{j=1}^{24} H_j \\ N_2 &= \sum_{j=1}^{23} H_j = \sum_{j=1}^{24} H_j - H_{24} = N_1 - H_{24} \end{aligned} \quad (6.2)$$

so that  $H_{24} = N_1 - N_2$ . Then in general:

$$H_j = N_i - N_{i+1} \quad (6.3)$$

where  $i = 25 - j$ . Equation 6.3 allows the raw counts read from the scalers to be converted into the number of hits measured in each time bin. The histogram of the number of times each bit was set  $N_i$  is called the integrated LTD spectrum while the histogram of hits in each time bin  $H_j$  is called the differential LTD spectrum.

The discussion above gives a simple overview of how the LTD generates a TOF histogram for each detector channel. In this example, there is just a simple input latch connected to two 16-bit shift registers (only 12 bits are used) which are clocked at 500 MHz and 180° out of phase with respect to each other. In reality, the LTD has added features that give it a well defined dead time, allow the user to monitor beam variations which may be helicity correlated and checks the integrity of the 500 MHz gated clock train. These features and others will be discussed in the sections below.

## 6.2 Gate Labels and Chip Placement

Before discussing specific features of the LTD module, it is useful to refer to specific gates (such as AND gates, latches, shift registers, etc.). Each gate on the LTD printed circuit board (and other custom North American modules) has a four character alphanumeric designator of the form GGCn. The first two characters (GG) refer to the type of gate (AN for AND gate, OR for OR gate, DL for D Latch, etc.). The third character refers to the chip number on the board for that type of gate. For instance, the LTD uses seven different D Latch chips, so DL3n would refer to the third D Latch chip. The fourth character (n) refers to the gate number on the chip. Often chips contain multiple gates, so n refers to the specific gate on chip C. Again, as an example, DL31 refers to D Latch chip 3, gate 1. Note that most chips start the gate numbering with 0. Some chips only contain one gate. In this case, Cn simply refers to the chip number. So, for instance, SR05 refers to shift register chip 5.

Table 6.3 lists all the types of chips used on the LTD along with the first three characters of their designator and the label they have on the printed circuit itself. Figure 6.2 shows the placement

Prefix	Chip Function	Gates	Board Label	Prefix	Chip Function	Gates	Board Label
AN1	AND gates	5	SY100E104 1	LR1	Line Receiver	5	SY100E116 1
AN2	AND gates	5	SY100E104 2	LR2	Line Receiver	5	SY100E116 2
BD1	Branch Driver	6	NS100323	OR1	OR gates	4	SY100E101 1
CD01	Clock Driver	1	SY100E111	OR2	OR gates	4	SY100E101 2
DL1	D Flip-Flop	4	SY100E131 1	OR3	OR gates	4	SY100E101 3
DL2	D Flip-Flop	4	SY100E131 2	PD01	Programmable Delay	1	SY100E195 1
DL3	D Flip-Flop	4	SY100E131 3	PD02	Programmable Delay	2	SY100E195 2
DL4	D Flip-Flop	4	SY100E131 4	PD03	Programmable Delay	3	SY100E195 3
DL5	D Flip-Flop	4	SY100E131 5	PD04	Programmable Delay	4	SY100E195 4
DL6	D Flip-Flop	4	SY100E131 6	QD1	Quad Driver	4	SY100E112
DL7	D Flip-Flop	4	SY100E131 7	SR01	Shift Register	1	SY100E141 01
DR1	D Register	6	NS100351 1	SR02	Shift Register	1	SY100E141 02
DR2	D Register	6	NS100351 2	SR03	Shift Register	1	SY100E141 03
DR3	D Register	6	NS100351 3	SR04	Shift Register	1	SY100E141 04
DR4	D Register	6	NS100351 4	SR05	Shift Register	1	SY100E141 05
DR5	D Register	6	NS100351 5	SR06	Shift Register	1	SY100E141 06
DR6	D Register	6	NS100351 6	SR07	Shift Register	1	SY100E141 07
DR7	D Register	6	NS100351 7	SR08	Shift Register	1	SY100E141 08
DR8	D Register	6	NS100351 8	SR09	Shift Register	1	SY100E141 09
				SR10	Shift Register	1	SY100E141 10

Table 6.3: A list of chips used on the LTD board and their function. The gate prefix is used in the diagrams below (6.2, 6.7, 6.6, 6.6, 6.6, 6.6, 6.8, 6.8). The first two characters designate the type of gate, the third character designates the chip number and a fourth number designates the gate number on that chip. So for instance, DL10 would be D Latch, chip 1 gate 0. For chips with only one gate, such as the shift registers, the third and fourth characters just refer to the chip number.

of the chips listed in table 6.3. The small dot on each chip indicates the position of pin 1. See figure D.1 for a diagram of the pins for the PLCC chips.

### 6.3 Next Pulse Neutralization (NPN)

The goal of the  $G^0$  experiment is to measure the helicity correlated asymmetry down to the level of 0.1 ppm. Therefore, accurate dead time corrections are critical. One way to achieve this is to make sure that the LTD board has a well defined dead time that is larger than the other modules in the electronics chain (see figure 1.1). Consider the dead time of the LTD in the simple discussion of the function above. Once the input latch is set, it cannot be set again till after it has been reset by the *STR* pulse. So if there are two hits on a given detector in a beam pulse, only the earliest one will set the input latch and thus be counted in the TOF histogram. All other hits in the beam

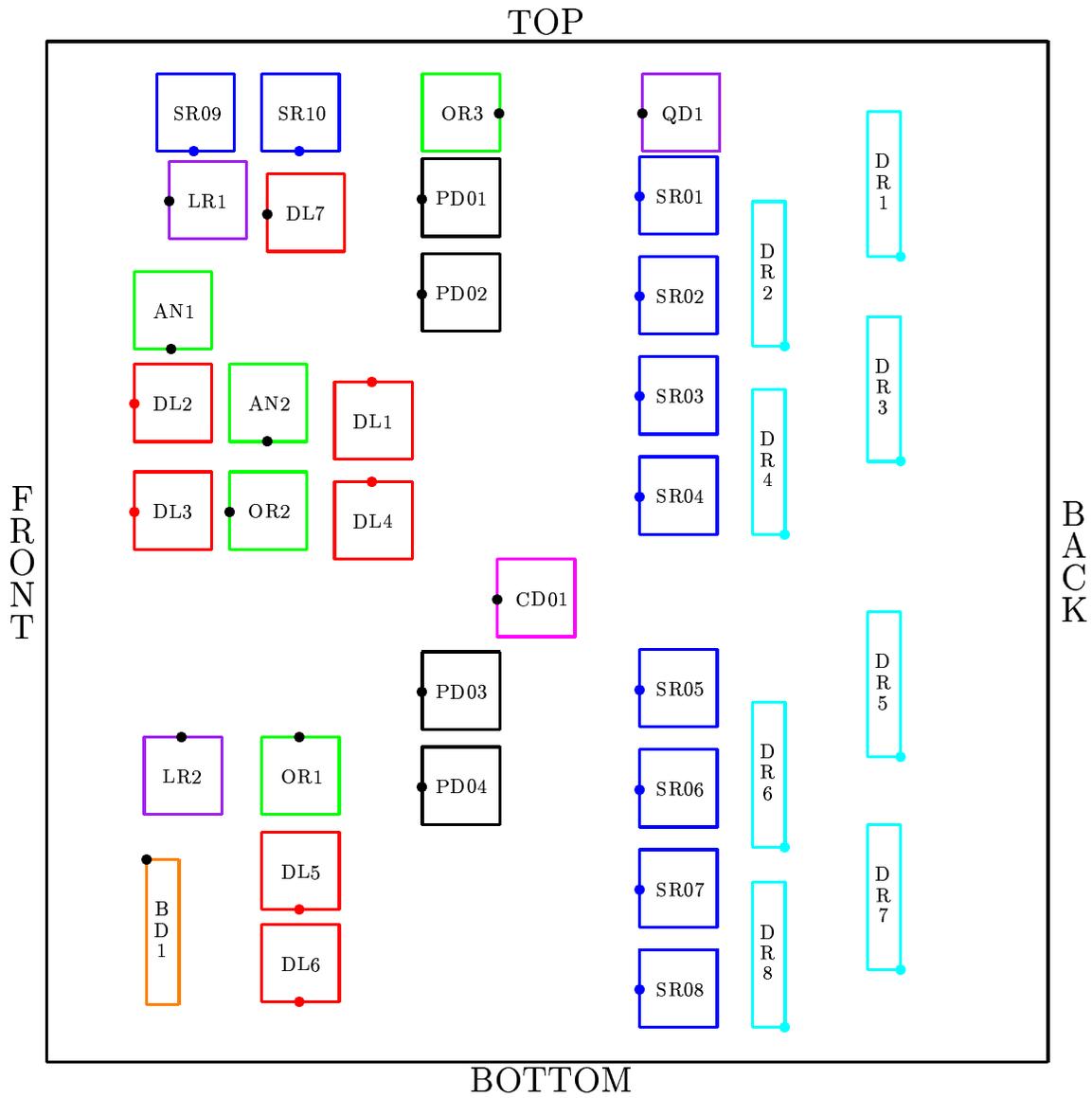


Figure 6.2: Chip positions for the LTD board. See table 6.3 for the meaning of the labels. The dots show the position of pin 1. See table D.1 for the pin arrangement of the PLCC chips.

pulse will be missed. Thus the input latch, and the LTD channel, will be dead from the time it is set till the end of the beam pulse. In this case, the dead time of the LTD will vary from 0 to 32 ns depending on the TOF of the particle. Early hits will produce a larger dead time than late hits. If a hit comes near the end of the beam pulse, the dead time of the LTD may well be shorter than the dead time of other components in the electronics chain and so the dead time of the whole system will be poorly defined. The LTD would be ready to take data, but some other module (such as the meantimer) would not. The exact time each module in the chain becomes live again after a hit may only be known to within a few ns. So it is impossible to make very precise dead time corrections.

For this reason, the LTD was designed with a feature called Next Pulse Neutralization (NPN) which gives the LTD a larger, but well defined, dead time. Basically the NPN system keeps the LTD dead for one full beam pulse after the beam pulse in which the latch was set. So if the latch is set in this beam pulse, the LTD will be dead for the remainder of this beam pulse and for the next beam pulse. The input latch is still reset at the end of this beam pulse, but the reset line is held high through the next beam pulse. As long as the reset line is high, the latch cannot be set and its output goes to 0. So, in the next beam pulse, the shift registers all clock in zeros. The effect of NPN is to make the dead time of the LTD range from 32 ns to 64 ns. Thus the upstream electronics will all have time to recover before the LTD is ready to take data again.

It is important to note that the NPN system can be set even when the reset of the input latch is being held high. Imagine there are two hits in consecutive beam pulses. The first hit sets the input latch and the NPN system ensures the LTD will be dead during the second beam pulse. When the second hit comes during that beam pulse, it will not set the input latch, so it will not be counted in the TOF histogram, but it will set the NPN. So the LTD will be dead for the third beam pulse too. Again, this is done to make sure the dead time of the LTD is greater than the dead time of the upstream electronics modules.

The NPN system is also set by either the front or back scintillator signals individually, even when they don't form a coincidence. Here again, the reason is to make sure the LTD has a larger dead time than the upstream electronics. So if the front scintillator fires, but not the back, the meantimer of the front scintillator would be dead but not the meantimer of the back scintillator. Thus, no coincidence could be formed at the LTD. Therefore, it is best to have the NPN set not just by coincidences but also by single hits. That way some channels of the upstream electronics won't be dead while the LTD is live. In the case of the back scintillator, the option of setting the NPN on single hits is jumper selectable. The back signal is set to be wider and to come earlier than the front signal. Therefore, for the earliest time bin, the back signal will come in one beam pulse while the front signal comes in the next. The back signal would then set the NPN making the LTD dead when the front signal arrived. For this reason, the jumper (BCK BUSY) connecting the back signal to the NPN should be open.

## 6.4 The Buddy System

Each LTD board has two input channels. The two detectors connected to these channels will have the same  $Q^2$  value but sit in opposite octants. Therefore the two detectors connected to one LTD module will be identical in design and should see nearly identical rates. The reason for this is so each LTD board can compare the rates on the two similar detectors to monitor the beam intensity

	Channel 1	Channel 2	Pulse
$B_{2p}$	busy	hit	previous
$B_{2s}$	busy	hit	same
$B_{1p}$	hit	busy	previous
$B_{1s}$	hit	busy	same

Table 6.4: A summary of the Buddy outputs, listed in the order of the output connector on the LTD.

fluctuations. This is referred to as the Buddy system and the two detectors going to one LTD are said to be Buddy detectors.

Call the two channels (detectors) 1 and 2. The Buddy system counts the number of times that one channel saw a hit when the busy was set on the other channel in the same beam pulse and when the busy was set on the other channel in the previous beam pulse. So for each of the two LTD channels, there are two Buddy counters for a total of four Buddy counters all together. These can be labelled as  $B_{1s}$ ,  $B_{1p}$ ,  $B_{2s}$ ,  $B_{2p}$  and are defined in table 6.4. As an example, say channels 1 and 2 both recorded a hit in the same beam pulse. In this case, both  $B_{1s}$  and  $B_{2s}$  would be incremented. Now say channel 1 records a hit in one beam pulse and channel 2 records a hit in the next beam pulse. In this case,  $B_{2p}$  would be incremented. If the channel 2 recorded a hit in the first beam pulse and channel 1 in the next, then  $B_{1p}$  would be incremented. As will be discussed in section 6.5, signals from either the front or back scintillators can set the NPN on a given LTD channel even if they don't form a coincidence and set the input latch. So, for instance, if the front scintillator on channel 1 fired, but not the back scintillator, then its NPN would be set. If channel 2 saw a hit (both front and back scintillators fired in coincidence) in that same beam pulse, then  $B_{2s}$  would be incremented but not  $B_{1s}$ .

The purpose of the Buddy system is to monitor the beam intensity fluctuations over time scales shorter than a macro pulse (1/30th of a second). If the beam intensity were fluctuating over many macro pulses, this would be apparent from the raw counts in each macro pulse. However, intensity fluctuations that are much shorter than a macro pulse would simply average out in the raw counts. So, for instance, if the beam intensity was oscillating by a few percent with a period comparable to several beam pulses (32 ns) there would be no way to distinguish this from a flat intensity just by looking at the raw macro pulse counts. However, the dead time corrections (see section 6.12) for the oscillating intensity would be different for the flat intensity. Now if the beam intensity was fluctuating for one helicity but not the other, this could lead to a false asymmetry. So it is important to have a way to monitor the beam intensity on time scales that are comparable to the length of the beam pulse.

The Buddy system allows us to monitor the beam intensity fluctuations within each macro pulse. To see this imagine if the beam intensity were absolutely flat, so the detector rates were constant. Then the two Buddy counters for a given channel would always be equal and  $B_{1p}/B_{1s} = B_{2p}/B_{2s} = 1$ . This just says the probability of one channel being dead when the other sees a hit is the same for every beam pulse. Now imagine a worst case where the beam intensity goes to zero every other beam pulse. In this case  $B_{1p} = B_{2p} = 0$  (since the intensity would be zero every other beam pulse, neither channel would see a hit when the busy of its Buddy was set in the previous

beam pulse) so that  $B_{1p}/B_{1s} = B_{2p}/B_{2s} = 0$ . Of course, the beam fluctuations do not need to be this extreme. Even fluctuations of a few percent between beam pulses or over many beam pulses would be apparent though the Buddy counts.

On the LTD itself, the Buddy system is comprised of four latches with their outputs connected to four AND gates (see section 6.5 and figure 6.5). Gates DL21 and DL31 (see section 6.2 for an explanation of the gate labels) hold the status of the input latches from the previous beam pulse for channels 1 and 2 respectively. Gates DL22 and DL32 hold the status of the busy (NPN) in the current beam pulse (having been set in the previous beam pulse). The AND gates AN10, AN11, AN12 and AN13 form the Buddy conditions listed in table 6.4 as shown in figure 6.5. The outputs of these AND gates go to the LTD front panel (see figure 6.11) where they are connected to scaler channels. Like the LTD time bits, these scaler channels are read out every macro pulse.

## 6.5 The Input Latches

Figure 6.5 is a block diagram of the input latch logic for the LTD module. It shows how the LTD input latches, the NPN system and the Buddy system all function. This section will describe these functions in detail. Note that individual logic gates will be referred to by the convention described in section 6.2. Each gate is labeled in figure 6.5 with gray lettering. The pin numbers for the inputs and outputs of each gate are also included with gray lettering. This will make the task of examining these signals with an oscilloscope probe much easier! Lines that directly involve the data signals (front and back scintillators plus the input latch signal) are drawn in red. Lines that carry the  $STR$  synchronization signal (see section 6.7) are drawn in blue and the  $\overline{STR}$  lines are drawn in green.

There are four basic sections to the input latch logic; the input latch itself, the busy system (NPN, section 6.3), the Buddy system (section 6.4) and a set of signal delays between the input latch and the even and odd shift registers. These delays are not currently used in the LTD modules, but since they are part of the design they will be discussed here for completeness. Only channel 1 and its gates will be discussed in this section, but note that channel 2 is nearly identical. Table 6.5 shows the gates which will be discussed for channel 1, the gates with the identical function in channel 2 and the logic category they fit into.

The input latch works in much the way it was described in section 6.1. The front and back scintillator signals come in through the DATA INPUTS connector on the front panel (see figure 6.11) as differential ECL signals. These go to line receiver gates LR10 and LR13 respectively. The outputs of these gates then go to the  $CLK$  and data input pins of latch DL11 respectively. The back signal is connected to the jumper BCK-GND. If BCK is selected, the back signal is connected to the data pin of DL11. If GND is selected, then the data pin is connected to ground and so the back signal is not required to make a coincidence. ECL levels are -1.7 V for 0 and -0.9 V for 1. Therefore ground at 0 V is always ECL 1. This allows testing of the LTD module without the requirement of a coincidence between the two input signals. For  $G^0$  running this jumper should be on BCK. Note that the back signal is also connected to the BCK BUSY jumper which will be discussed below with the busy system.

The reset of the input latch is connected to the jumper NPN-STROBE. With the jumper on NPN, the reset comes at the end of the beam pulse and is held through the next beam pulse if the

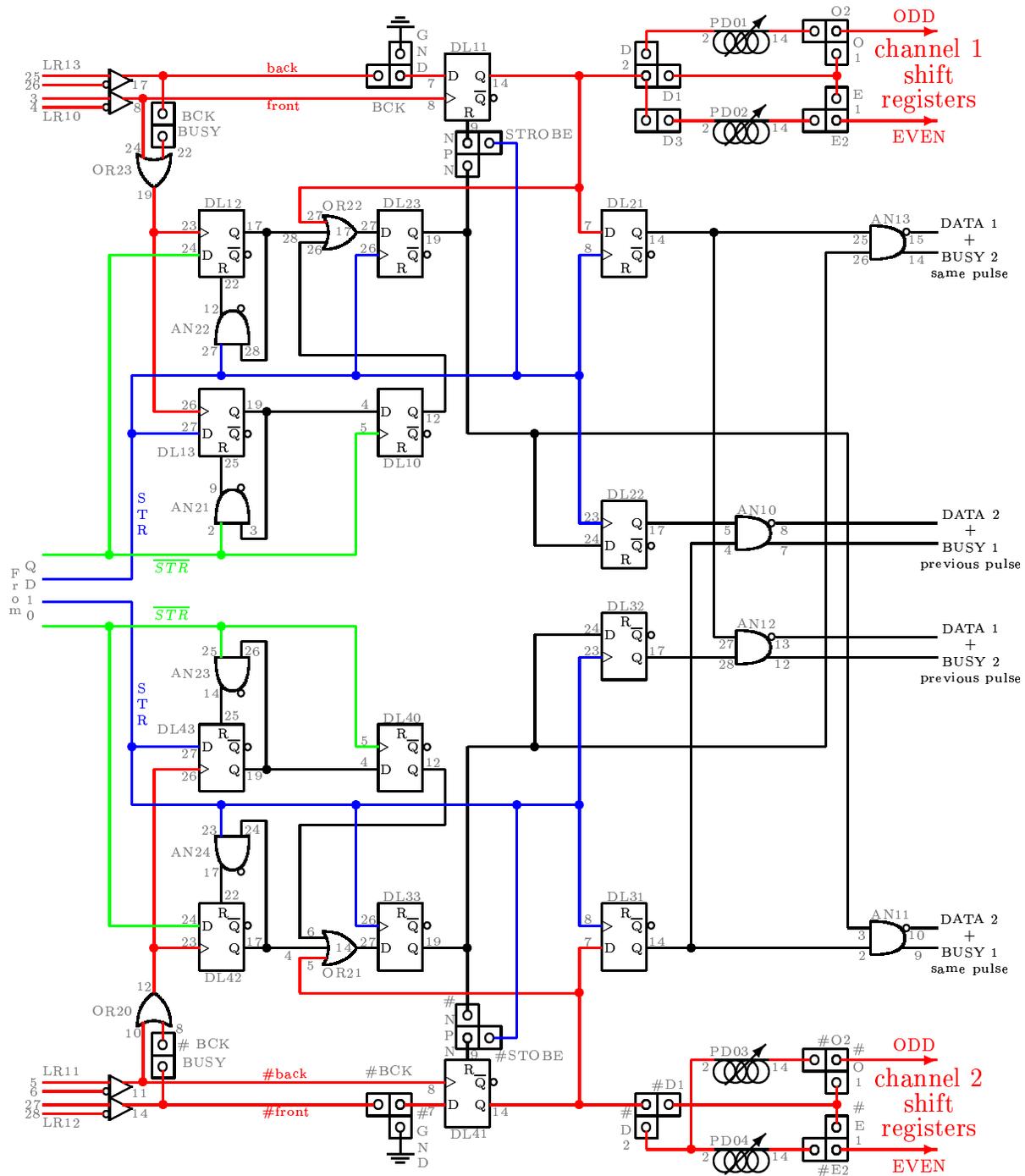


Figure 6.3: Block diagram for the LTD input latches and Buddy logic. The detector signal paths are in red, the  $\overline{STR}$  lines are blue and the  $\overline{STR}$  lines are green.

Channel 1 Gate	Channel 2 Gate	Function
DL11	DL41	Input latch
PD01	PD03	Signal delay to Odd shift registers
PD02	PD04	Signal delay to Even shift registers
DL12	DL42	NPN, singles monitoring, <i>STR</i>
DL13	DL43	NPN, singles monitoring, <i>STR</i>
DL10	DL40	NPN, singles monitoring, <i>STR</i>
DL23	DL33	NPN, status
OR23	OR20	NPN, singles monitoring
OR22	OR21	NPN, status
AN22	AN24	NPN, singles monitoring, <i>STR</i> reset
AN21	AN23	NPN, singles monitoring, <i>STR</i> reset
DL21	DL31	Buddy, input latch status
DL22	DL32	Buddy, NPN status
AN13	AN11	Buddy, $B_{1s}$ and $B_{2s}$
AN12	AN10	Buddy, $B_{1p}$ and $B_{2p}$

Table 6.5: The gates used for the input latch logic for channel 1 and channel 2 as shown in figure 6.5.

NPN system is activated. This will be discussed below. With STOBE selected, the latch is reset by the *STR* signal. Therefore it will be reset briefly at the end of each beam pulse and will not be effected by the NPN system at all. For  $G^0$  running, this jumper should be on NPN.

The output of the latch DL11 ultimately goes to the data inputs of the even and odd shift registers. First it connects to jumper D1-D2. If D1 is selected, the output will go to the jumpers O1-O2 and E1-E2. Here, both O1 and E1 should be selected which send the signal to the data inputs of the odd (SR01) and even (SR03) shift registers respectively. If D2 is selected, then D3 must also be selected. In this case, the latch signal will go to two different programmable delay gates (PD01 and PD02). The delay of each gate is set with an 8-bit DIP switch with values that range from 0 ps to 2560 ps in 20 ps steps. There is also a fixed internal delay of the chip which is about 1400 ps. This will be important when discussing the jumpers in section 6.7. The purpose of these delay gates was to provide an adjustment for the arrival time of the signal at the even and odd shift registers individually.

By design, the LTD board should clock these shift registers  $180^\circ$  out of phase. However, in practice, this phase difference can be as much as  $180^\circ \pm 20^\circ$  which leads to widths which are different for even and odd time bins. This even-odd effect will be discussed in more detail in section 6.6. The programmable delay gates were included as a jumper selectable option in the hopes of nulling out this even-odd effect by adjusting the signal arrival time. For instance, if the even clock ( $\overline{CLK}$ ) signal is slightly ahead of the odd clock  $CLK$ , then the odd bins will be slightly thinner than the even bins. If however, the input latch signal arrives at even shift register the slightly before it arrives at the odd shift register, then both even and odd bins would be equal again. Unfortunately this scheme did not work as expected in tests of the LTD, so the gates PD01, PD02, PD03 and PD04 are not used and jumpers D1, O1 and E1 are hardwired. In fact, the LTD boards were manufactured with these jumpers set by traces on the outer layer. For one LTD board we scratched these traces

so we could set jumpers D2, D3, O2 and E2 and test the delays. On all other LTD boards, these delays are by-passed as the default.

The output of DL11 also connects to latch DL21 and OR gate OR22. Latch DL21 is part of the Buddy system, it holds the status of DL11 from the previous beam pulse. OR22 is part of the NPN system taking the OR of three signals which can set the NPN during a beam pulse. This will be discussed in more detail below.

The NPN system gives the LTD an extended, but well defined, dead time so that dead time corrections will be as accurate as possible (see section 6.3). Basically this system holds the reset on the input latch for the duration of the beam pulse after it was set. It is set by either a coincidence of the front and back scintillator signals or by single hits on the front scintillator (and back scintillator if the BCK BUSY jumper is closed).

Looking at figure 6.5, the front and back (if BCK BUSY is closed) signal lines are connected to OR gate OR23. The output of this gate goes to the clock input for latches DL12 and DL13. These two latches work together to monitor the front and back and signal lines through the whole beam pulse. The data line of DL12 is connected to the  $\overline{STR}$  pulse and the data line of DL13 is connected to the  $STR$  pulse. So the data line of DL12 will be high when the data line of DL13 is low and vice versa. The reset line of DL12 is connected the output of the AND gate AN22. The inputs of this gate are the  $STR$  pulse and the output of DL12. So DL12 will be reset with the  $STR$  pulse but only if it is already set. Likewise, the reset of DL13 is connected to AN21 which has the inputs of  $\overline{STR}$  and the output of DL13. So DL13 will be reset with the  $\overline{STR}$  pulse but only if it is already set. From this arrangement it follows that DL12 can be set while DL13 is being reset and DL13 can be set while DL12 is being reset. This is done to completely cover the beam pulse. If only one latch had been used, say DL12, then hits coming during the  $STR$  pulse would fail to trigger the NPN since the latch cannot be set while its reset is held high.

At the end of the  $STR$  pulse, the status of DL13 is shifted into DL10 and DL13 is reset (if it was set). DL10 is clocked by  $\overline{STR}$  with the output of DL13 connected to its data input. So on the rising edge of  $\overline{STR}$  (which is the falling edge of  $STR$ ) the status of DL13 is moved into DL10. The output of DL10 goes to OR22. The output of DL12 is connected directly to OR22 as is the output of DL11 (the input latch).

The end of a beam pulse is marked by the rising edge of the  $STR$  pulse. Since DL23 is clocked by the  $STR$  pulse, this is the time its output will go high if DL11, DL12 or DL10 was set in the previous beam pulse. The output of DL23 is connected to the reset of DL11 through the jumper NPN-STROBE and is thus what determines the status of the NPN system. If the NPN was set during the previous beam pulse, then the output of DL23 will be high in this beam pulse. DL23 is not reset by any pulse, it simply clocks in either a 1 or 0 depending on the status of OR22 on the rising edge of  $STR$ . Note that DL13 is connected to DL10 and not OR22. This is because DL13 monitors the single hits during the time  $STR$  is high, so it covers the first few ns (width of  $STR$ ) of a beam pulse. DL12 covers the period after  $STR$  till the end of the beam pulse.

The Buddy System (see section 6.4) uses the status of various latches from both LTD channels. The Buddy outputs (on the front panel of the LTD module) come from the AND gates AN10, AN11, AN12 and AN13 as shown in figure 6.5. At the end of a beam pulse, the status of DL11

(the input latch for channel 1) is moved into DL21 and the status for DL41 (the input latch for channel 2) is moved into DL31. At the same time the status of the channel 1 NPN is moved into latch DL22 while the status of the channel 2 NPN is moved into latch DL32. The inputs for AN10 are the status of DL22 (channel 1 NPN from the previous pulse) and the status of DL31 (channel 2 input latch from the previous pulse). So AN10 gives  $B_{2p}$ . The inputs for AN11 are the status of DL23 (channel 1 NPN for the current pulse) and the status of DL31 (channel 2 input latch from the previous pulse). So AN11 gives  $B_{2s}$ . The inputs for AN12 are the status of DL21 (channel 1 input latch from the previous pulse) and the status of DL32 (channel 2 NPN from the previous pulse). So AN12 gives  $B_{1p}$ . The inputs for AN13 are the status of DL21 (channel 1 NPN from the previous pulse) and the status of DL33 (channel 2 NPN for the current pulse). So AN13 gives  $B_{1s}$ .

## 6.6 The Time Digitization

In figure 6.1, the input latch is connected to two 16-bit shift registers. In reality, the output actually goes to two pairs of 8-bit shift registers. Within the pairs, the last bit of one shift register acts as the input for the second shift register. So the the first shift register holds the first 8 bits of the bit pattern and the second shift register holds the last 8 bits. In fact, there are only 12 clock pulses going to each pair, so the second shift register only holds the last 4 bits, for a total of 12. One pair of shift registers is clocked on  $CLK$  so these are called the odd shift registers (because they see rising edges 1, 3, 5, ...). The other pair of shift registers is clocked on  $\overline{CLK}$  so these are called the even shift registers (because they see rising edges 2, 4, 6, ...). Block diagrams are shown for the top-odd, top-even, bottom-odd and bottom-even shift registers in figures 6.6, 6.6, 6.6 and 6.6 respectively.

At the end of each beam pulse, during the time the clock is gated off (see section 6.1), the shift register bit pattern is copied into D registers. There are a total of 12 D register gates for each shift register pair, corresponding to the 12 bits. Each bit is copied into one D register. Basically a D register is just a latch. The data input is connected to the bit output from the shift register. The clock input on all the D registers is connected to the synchronization signal  $STR$  (see section 6.7 and figure 6.7) which comes after the last clock pulse. On the rising edge of  $STR$  the D registers all read in the status of their shift register bit. The outputs of these D registers ultimately go to the scalers. After their bit pattern has been copied to the D registers, the shift registers are cleared by the  $CLR1$  pulse and are thus ready for the next beam pulse. The D registers are cleared in the middle of the next beam pulse (roughly 16 ns) later by the  $CLR2$  pulse. Since the D registers are all set at the same time and then later all cleared at the same time, they produce pulses of a fixed width which is relatively long. This ensures the LTDs produce robust output pulses which won't be missed by the scalers.

### 6.6.1 The Data Blind Spot

Out of the 24 LTD time bins, 23 are determined entirely by the edges of the gated clock train. Looking at figure 6.6.1, the width of the second time bin is determined by the first rising edge of  $CLK$  and the first rising edge of  $\overline{CLK}$ . The width of the third bin is determined by the second rising edge of  $\overline{CLK}$  and second rising edge of  $CLK$ , and so forth. The first bin, however, starts from the rising edge of the  $STR$  pulse (see sections 6.5 and 6.7) and ends with the rising edge of

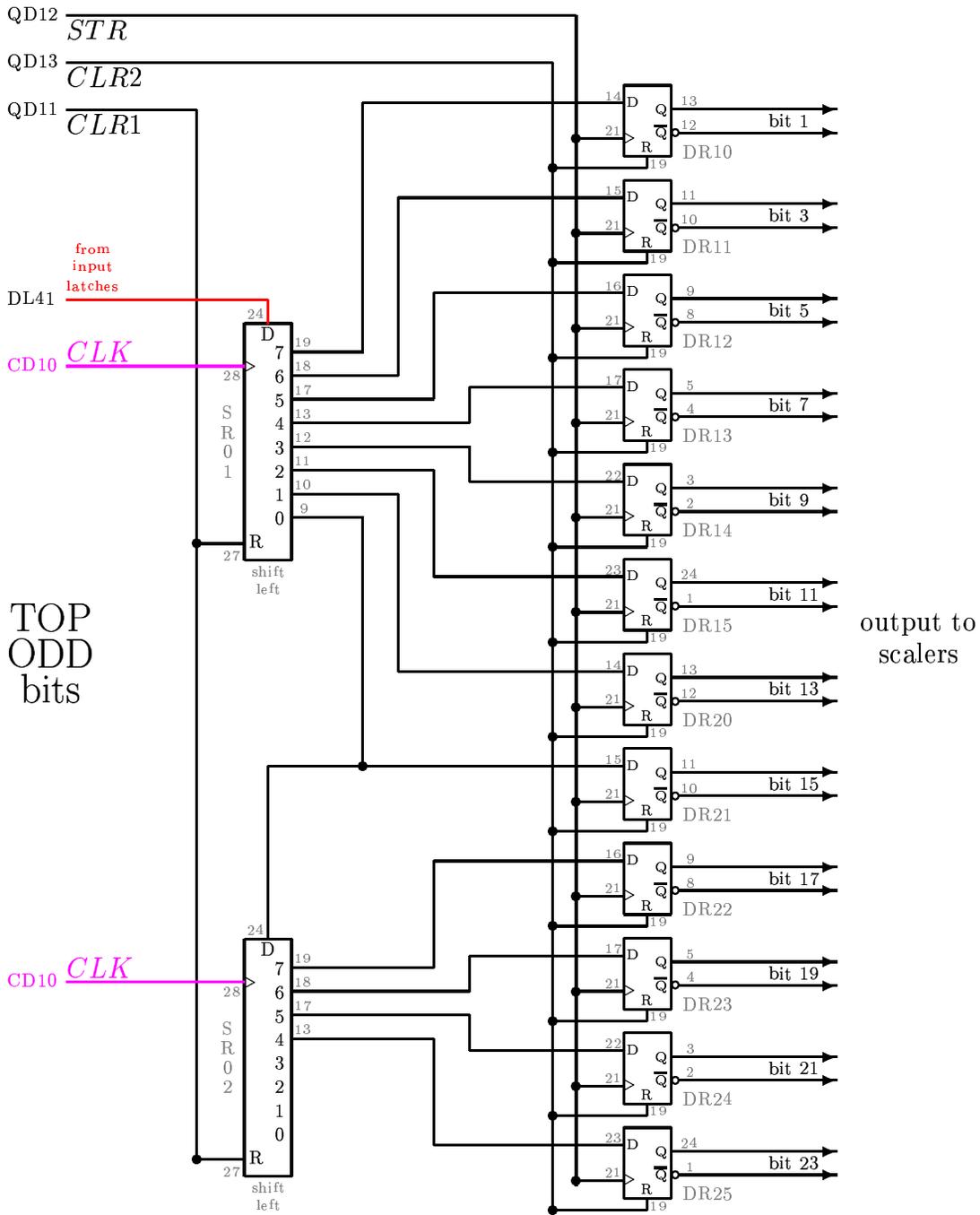


Figure 6.4: Block diagram for LTD top channel, odd shift registers and D register outputs.

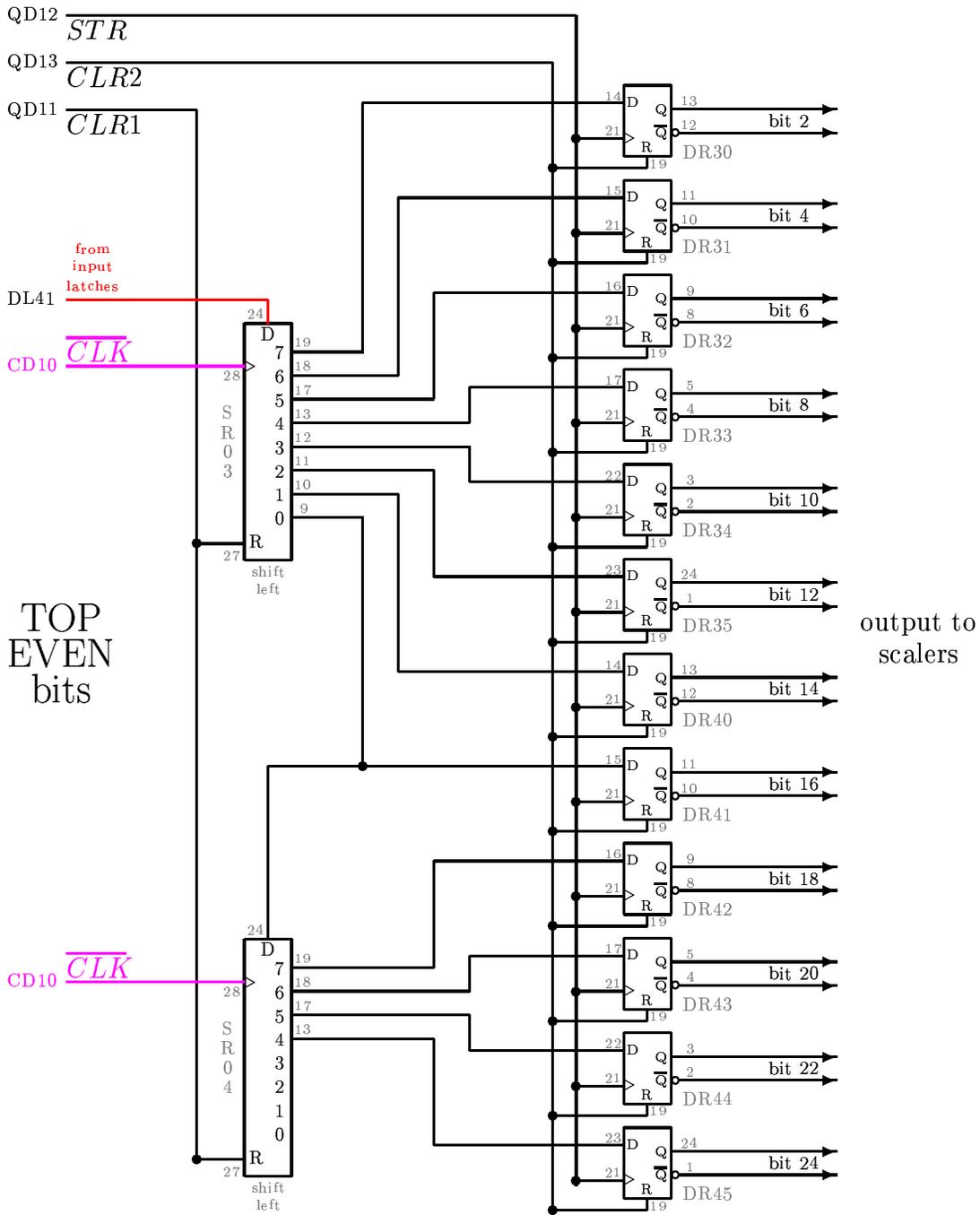


Figure 6.5: Block diagram for LTD top channel, even shift registers and D register outputs.

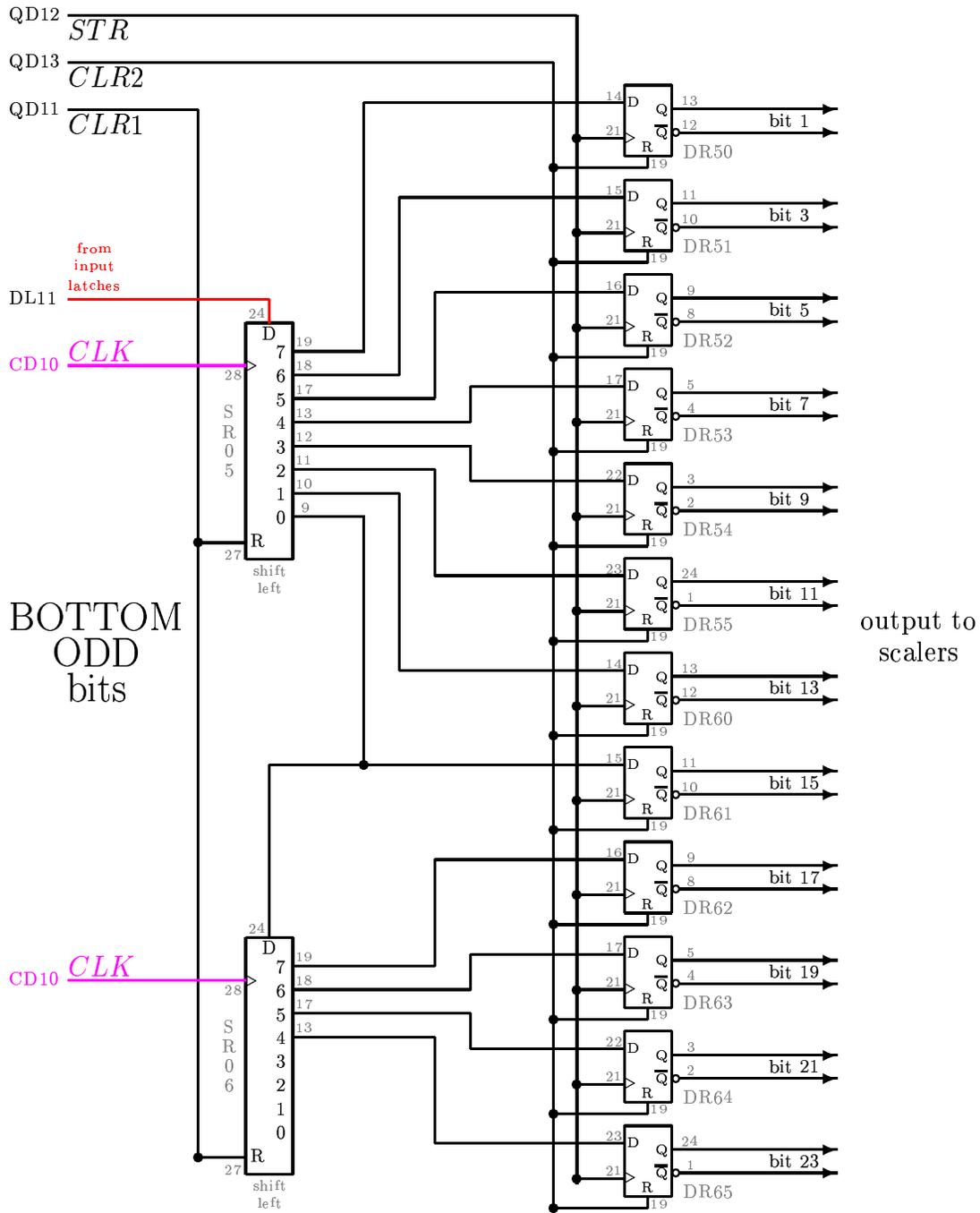


Figure 6.6: Block diagram for LTD bottom channel, odd shift registers and D register outputs.

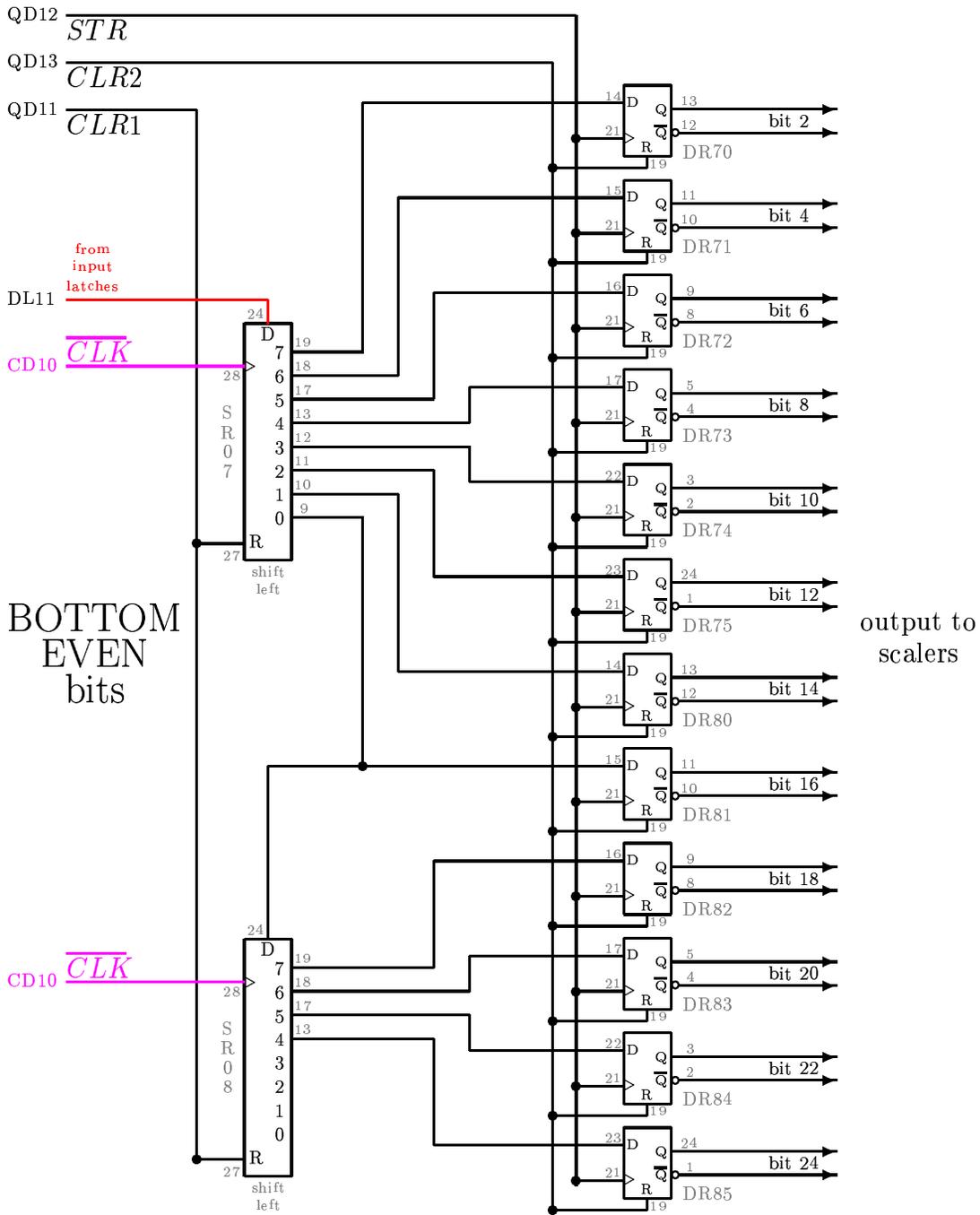


Figure 6.7: Block diagram for LTD bottom channel, even shift registers and D register outputs.

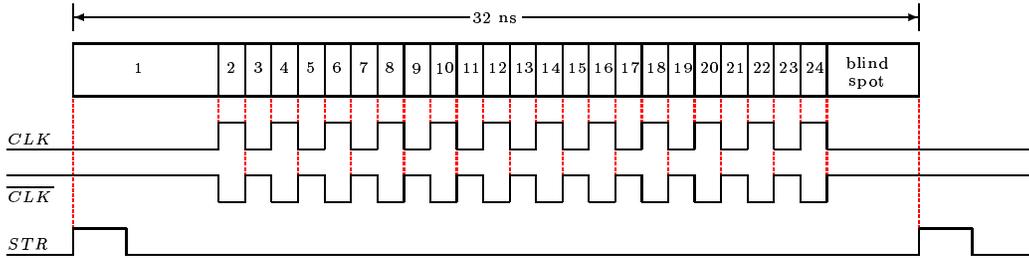


Figure 6.8: A graphical depiction of the LTD data blind spot. The width of time bin 1 (bit 24) is from the rising edge of  $STR$  at the input latches (see figure 6.5) till the first rising edge of  $CLK$ . This is about 6.5 ns. The widths of time bins 2 to 23 are just determined by the successive edges (rising and falling) of the 500 MHz clock, so they are nominally 1 ns wide. Any hits that come after the last clock edge and before the rising edge of  $STR$  will be lost. They will set the input latch but this will be reset by  $STR$  before the clock train starts. Therefore, hits that come during this period will not get shifted into the shift registers.

the first  $CLK$  pulse. At the end of the beam pulse, after the last rising edge of  $\overline{CLK}$ , it is possible for hits to set the input latch. However this latch will be reset (and the NPN set for the next beam pulse) on the rising edge of  $STR$ . Therefore, hits that come in this period, after the last clock pulse and before  $STR$  will not get shifted into the shift registers. This is referred to as the LTD blind spot.

The  $STR$  pulse timing is set by counting clock pulses in the gated clock train (see section 6.7). So it comes at a fixed time relative to the gated clock train. On average  $STR$  arrives at the input latches about 2.5 ns after the last clock pulse. Thus the size of the LTD blind spot is about 2.5 ns wide. Note that the NPN system is not blind here, so hits in this time will set the NPN, they just won't be counted in the TOF histograms. The proton peak (forward running) should fall much earlier than the blind spot, so losing hits in this region won't degrade the TOF measurement. However, information on the background will be lost which is important to the dead time corrections (see section 6.12). The FASTBUS system (see chapter 12) will monitor the entire beam pulse spectrum albeit with lower resolution than the LTDs. So information about the background rates lost by the blind spot will be available from the FASTBUS data.

## 6.6.2 The Even-Odd Effect

Nominally, the even and odd shift registers should be clocked  $180^\circ$  out of phase with respect to each other. This is due to the fact that the odd shift registers are clocked by  $CLK$  and the even shift registers are clocked by  $\overline{CLK}$ , which is the complement of  $CLK$ . The gated clock train is provided to the LTD board by the KGB board (see chapter 4). The signal goes to a clock driver chip (CD01) which makes nine differential ECL copies (nine copies of  $CLK$  and nine copies of  $\overline{CLK}$ ). These copies are then distributed to the shift registers. The trace lengths for the copies on the board were carefully laid out to all have the exact same length to maintain the  $180^\circ$  phase difference. Even so, the phase difference has varied channel to channel by as much as 10%. The reasons are likely due to variations in the shift registers chips themselves and other effects.

Variations in the phase difference between even and odd shift registers has an effect on the time

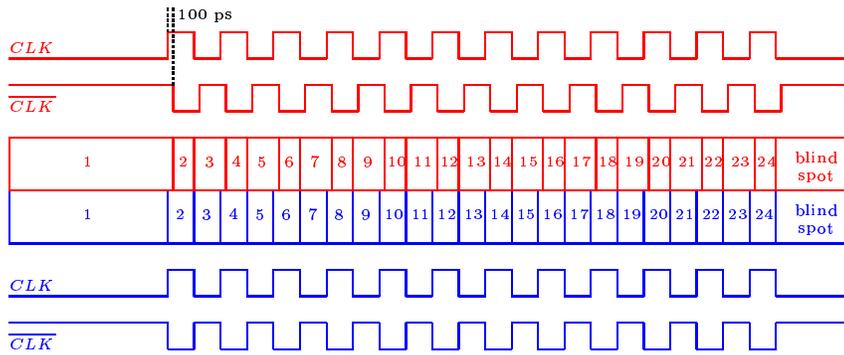


Figure 6.9: A graphical depiction of the LTD even-odd effect. Ideally the even and odd shift registers should be clocked  $180^\circ$  out of phase as in the bottom representation where both  $CLK$  and  $\overline{CLK}$  are shown in blue. The positions of the rising edges are indicated just above with vertical lines making boxes which show the nominal time bin widths. Most of the widths, with the exception of the first and the blind spot are 1 ns wide. Above this, both  $CLK$  and  $\overline{CLK}$  are drawn again in red but now with  $\overline{CLK}$  coming 200 ps later. Now the even bin widths are 0.8 ns and the odd bin widths are 1.2 ns.

bin widths as shown in figure 6.6.2. If  $CLK$  and  $\overline{CLK}$  are exactly  $180^\circ$  out of phase, then the widths of bins 2 to 24 will be exactly 1 ns (as shown in blue in the bottom of the figure). Now imagine that  $\overline{CLK}$  comes a little later, say 200 ps, than  $CLK$ . In this case, the odd bin widths will be 1.2 ns and the even bin widths will be 0.8 ns (as shown in red in the top of the figure). This is referred to as the even-odd effect.

This effect shows up most clearly in the case of a flat time spectrum. If a LTD channel is connected to a random signal (such as a scintillator viewing a radioactive source), the rate would be constant for all time bins. Therefore the number of hits in each time bin would be proportional to its width. So the TOF spectra would look like figure 6.6.2 where the odd bins are 20% higher than the even bins. In this figure, the number of hits in each time bin has been normalized to the average number of hits per bin. If there were no even-odd effect, each bin would have a height of 1 on the plot. Instead, bins 2 to 24 (bin 1 is not included since it is much larger than the nominal 1 ns) vary in height, such that the even bins are 1.2 and the odd bins are 0.8. On the actual LTD boards, this difference was more like  $\pm 10\%$  but it has been drawn here as  $\pm 20\%$  to correspond with figure 6.6.2.

The even-odd effect was measured for each LTD channel after construction using the method above. Namely, a random signal from a scintillator viewing a radioactive source was input to each channel. The rate was kept low so that dead time effects would be negligible. A plot much like figure 6.6.2 was generated to determine the magnitude and sense of the phase difference. Then a small capacitance (a few pF) was placed on either the  $CLK$  or  $\overline{CLK}$  lines going to the shift registers. This had the effect of slowing down the rising edge of the pulses for that signal, making them cross the ECL transition voltage (-1.3 V) a little later than they normally would. So those shift registers (either even or odd) shifted a little later than the opposite pair. This reduced the even-odd effect to the  $\pm 10\%$  mentioned above.

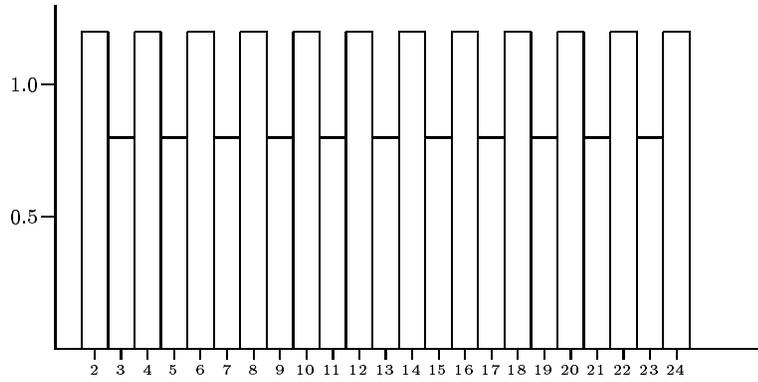


Figure 6.10: An example of a TOF histogram for LTDs with random signal inputs and with 20% even-odd effect. Since the rate is flat, the number of counts in each time bin is proportional to the width of the bin. Here the number of counts in each bin has been normalized to the average number of counts per bin. Time bin 1 is not included since its width is much greater than the nominal 1 ns.

### 6.6.3 Bin Width Variations

In addition to the even-odd effect, there are other bin by bin variations in the LTD bin widths. There are many different factors which affect these variations (such as changing the KGB parameters (chapter 4) or differences in the shapes of  $CLK$  and  $\overline{CLK}$ ), but generally they are stable over short time periods such as a few days. However, over long periods of time the variations will drift. Therefore it is useful to measure them from time to time.

Measuring the bin widths can be done with the method described above. That is, create a random signal by having a PMT with scintillator view a radioactive source. The signal should be low rate to keep dead time effects negligible. This signal can be fed into each LTD channel for some period of time (say a few hours at a few kHz). The result will be a histogram of the time bins where the number of counts in each bin is proportional to the width of the bin. This is called the white noise method of measuring the bin widths.

During the running of  $G^0$ , the bin widths will be measured periodically with the Grey Noise Box (GNB) (see chapter 10). This box produces a white noise signal by shining a LED on a PMT rather than a scintillator viewing a radioactive source (as described above), but the result is the same. The output of the GNB will go to the White Noise Fanout module (WNF) (also see chapter 10) which makes enough copies of the signal to feed into 16 (1 crate) LTDs. The outputs of the WNF are the same as the outputs of the meantimers. So the cables from the meantimers to the LTDs can be moved, at the meantimer end, over to the WNF. Measurement of the LTD bin widths in this fashion should be performed once or twice a week while the experiment is taking beam.

## 6.7 The Synchronization Signals

During each beam pulse, there is a great deal of actions that must take place. The input latches must be reset (along with setting NPN and Buddies), the shift register outputs must be copied to the D registers and then the shift registers must be reset, then eventually the D registers must also be reset. All this activity has to be coordinated somehow. For this reason, the LTD generates

several synchronization signals during each beam pulse. Basically, these are generated by counting the number of clock pulses in the gated clock train and creating the signals at the appropriate times.

There are three synchronization signals which are  $STR$  (and  $\overline{STR}$ ),  $CLR1$  and  $CLR2$ . The  $STR$  and  $\overline{STR}$  signals are used to clear the input latches and set the NPN busy for the next beam pulse (see figure 6.5). The  $STR$  signal is also used to strobe the D registers. That is, it goes to the clock inputs on the D registers to tell them when to copy over the shift register bits. The  $CLR1$  signal clears the shift registers after their outputs have been copied into the D registers. Therefore,  $CLR1$  must come a few ns after  $STR$ . The last signal,  $CLR2$ , clears the D registers in the next beam pulse. Therefore, it actually comes a little into the next beam pulse. The function of  $STR$ ,  $CLR1$  and  $CLR2$  may be seen in figures 6.6, 6.6, 6.6 and 6.6.

The generation of the LTD synchronization signals is shown in figure 6.7. The two shift registers SR09 and SR10 are both connected to either  $CLK$  or  $\overline{CLK}$ . The choice of  $CLK$  or  $\overline{CLK}$  is made with the jumpers SYNC CLK and TERMINATE (not shown on the diagram). SYNC CLK has three pins and selects  $CLK$  if the jumper is on the left (where the front panel of the module is on the left) or  $\overline{CLK}$  if the jumper is on the right. TERMINATE also has three pins and should always be on the opposite side of the jumper on SYNC CLK. The reason is that all unused outputs of the clock driver chip (CD01) are pulled down for stability. If  $CLK$  is used, then TERMINATE should be on the opposite side to connect  $\overline{CLK}$  to a pull down resistor. Likewise, if  $\overline{CLK}$  is used, then TERMINATE should be set to  $CLK$ . The data line of SR09 is connected to ground (effectively ECL high), so it always shifts in ones. The data input of SR10 is connected to the last output bit of SR09, so the two shift registers function together as one big 16-bit shift register. SR09 and SR10 are reset by the  $SYNC$  pulse, which is externally input to the board.  $SYNC$  comes every 32 ns and is generated at the KGB (see chapter 4) from the  $YO$  pulse. In addition to resetting SR09 and SR10, it also acts as an external marker for the end of the beam pulse. As such, it should not be confused with  $STR$  which defines the start of the beam pulse for the input latches.  $STR$  is generated on the LTD board and is timed by the clock train, while  $SYNC$  is generated externally and is timed by  $YO$ .

Since SR09 shifts in a 1 for every clock pulse of  $CLK$ , each output bit corresponds to a fixed time within the beam pulse. Table 6.7 shows how these bits are used. This will be useful in the discussion of the synchronization signals below. Alongside the number of clock pulses in table 6.7 is the time within the beam pulse. This time is measured from when the  $STR$  signal reaches the input latches (thus defining the start of the beam pulse). Thus the first clock pulse actually comes about 6.5 ns into the beam pulse. A total of 16 bits are listed in table 6.7 even though there should only be 12 pulses in the clock train. Some of these extra bits are used to check for errors in the clock train (see section 6.8). The discussion below will focus on the synchronization signals in the order in which they are generated in the beam pulse.

The third clock pulse (bit 5 of SR09) sets the latch DL62, which is then reset by the fifth clock pulse (bit 3 of SR09). This creates a pulse that is about 4 ns long 10-11 ns into the beam pulse. The output of DL62 goes to the quad driver QD13 which makes two copies. This is the  $CLR2$  signal which is used to clear the D registers (see figures 6.6, 6.6, 6.6 and 6.6). Due to propagation delay between DL62 and the D registers,  $CLR2$  doesn't actually clear them till about 14-16 ns into the beam pulse.

Clock pulse 8 sets output bit 0 on SR09 which is connected to jumper S16. Bit 0 is also con-

connected to the data input of SR10, so the two shift registers act as one. Clock pulses 9, 10, 11 and 12 set bits 7, 6, 5 and 4 on SR10 which are connected to jumpers S18, S20, S22 and S24 respectively. These jumpers (S16 to S24) are used to set the timing of the *STR* and *CLR1* signals. The other side of these jumpers are all connected to the clock input of latch DL72. So if, for instance, jumper S20 is selected, then the 10th clock pulse would set DL72. The outputs of DL72 creates several different pulses. The *Q* output goes to the quad driver QD10 which makes to normal copies and two inverted copies. These are the *STR* and  $\overline{STR}$  signals respectively used by the input latches. The *Q* output also goes to the STR WIDTH jumper. If the top two pins are selected, then the *Q* output of DL72 is connected directly to its reset. From propagation delay of the signal paths, this gives *STR*,  $\overline{STR}$  and *CLR1* a width of about 2 ns. The  $\overline{Q}$  of DL72 goes to QD12 through the jumper STR DELAY. QD12 makes two inverted copies of the  $\overline{Q}$  output (which means the copies will be identical to just *Q*) which is just the strobe (*STR*) signal for the D registers (see figures 6.6, 6.6, 6.6 and 6.6). The jumper STR DELAY was included on the LTD board for use with the programmable delays discussed in section 6.5. Due to the internal propagation time of the programmable delay chips, the *STR* and *CLR1* signals going to the D registers had to be delayed an additional 2 ns. So the bottom half of this jumper includes a 2 ns trace length delay. The programmable delay chips are not implemented on the LTD, so a jumper should only be placed across the top two pins of STR DELAY.

The  $\overline{Q}$  output of DL72 also goes to a series of four OR gates. In order, these are OR33, OR32, OR31 and OR30. The outputs of these gates go to the jumpers C1, C2, C3 and C4 respectively. In turn, the other side of these jumpers go to the jumper of STR WIDTH and to QD11 through the jumper CLR1 DELAY. QD11 makes two copies of *CLR1* which clear the shift registers SR01 to SR08 (see figures 6.6, 6.6, 6.6 and 6.6). Like STR DELAY, CLR1 DELAY was included to compensate the arrival time of *CLR1* at the D Registers for the internal propagation time of the programmable delay chips. This jumper should be set to connect directly to QD11. Signals from the jumpers C1, C2, C3 and C4 will differ in time by the propagation time of each OR gate, which is about 300-500 ps. Therefore, these jumpers select the amount of time that *CLR1* comes after *STR* in roughly 500 ps steps. Since these jumpers are also connected to STR WIDTH, if the jumper is on the bottom two pins, then the DL72 will not be reset till the time of *CLR1*. This would result in a much wider *STR* pulse. It was thought that resetting DL72 with its own output could result in a *STR* pulse so thin it would be unuseable. In fact, as mentioned above, *STR* is about 2 ns wide, so this option is not necessary.

## 6.8 Clock Train Errors

The function of the LTD depends on receiving a clock train from the KGB (see chapter 4) with 12 clock pulses (each 2 ns apart) followed by an 8 ns gate. If the number of pulses in the clock train is less than 12 or more than 12, the LTD would not function properly. For instance, if the clock train only had 11 clock pulses, then output bits 23 and 24 would never be set. Early hits would be shifted across to bit 22 and then stop. If there were 13 clock pulses, then data would be lost as the earliest hits would shifted past bit 24. If the number of clock pulses was significantly different than 12, it could cause some synchronization signals to be generated at the wrong time or not generated at all.

For these reasons, the LTD counts the number of clock pulses in each clock train to be sure there are exactly 12. If the number is anything other than 12, it generates an error signal. Also, the LTD checks to make sure that a *SYNC* signal came during each beam pulse. Therefore, there are three

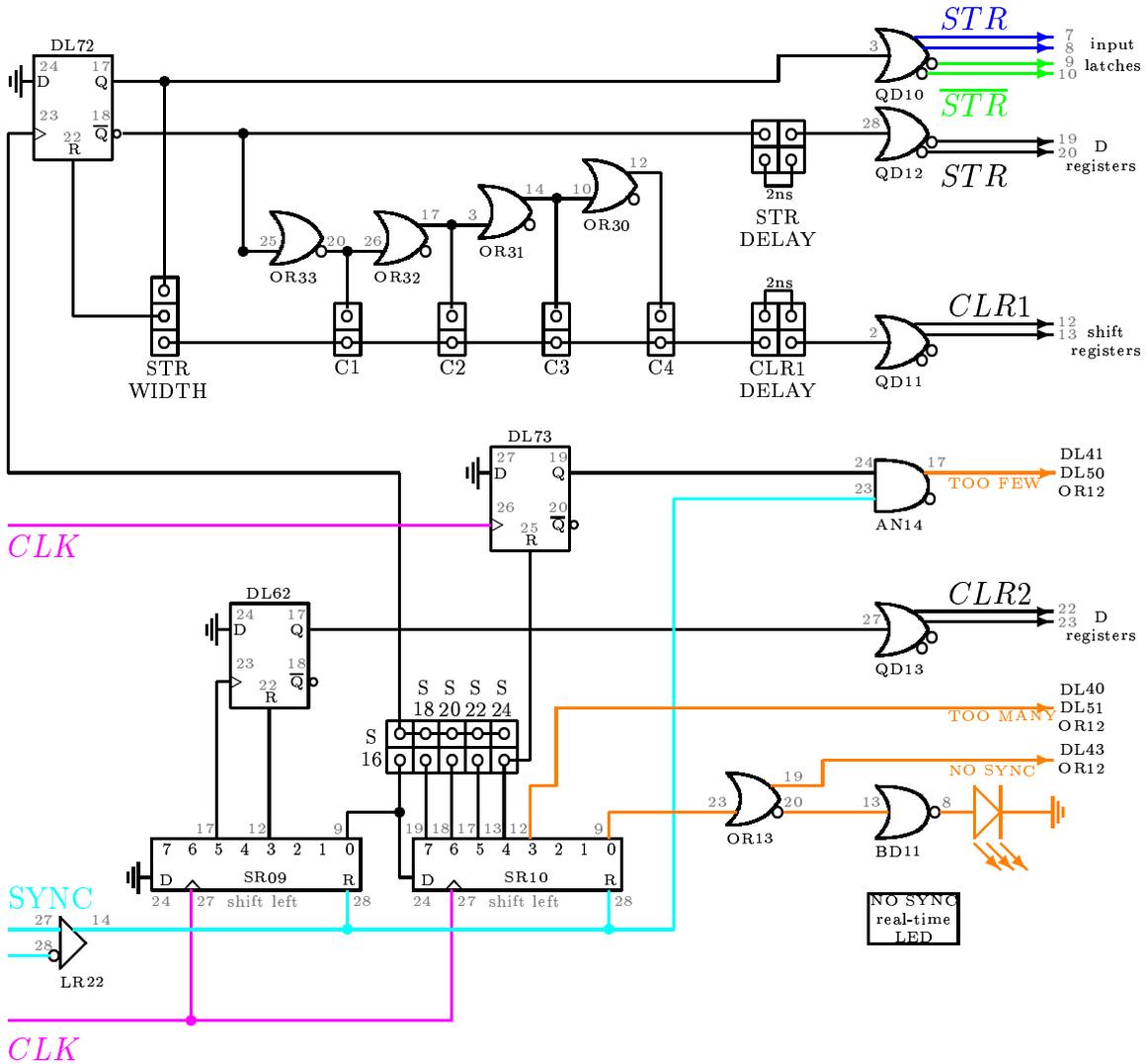


Figure 6.11: Block diagram for the LTD synchronization signals. The shift registers (SR09 and SR10) count the clock pulses in the clock train (magenta) and produce the strobe and clear pulses. The strobe pulses ( $STR$ ) go to both the input latches (see figure 6.5, blue is for the  $STR$  signal and green is for the  $\overline{STR}$  signal) and the D registers.  $CLR1$  clears the shift registers after they have been strobed.  $CLR2$  clears the D registers in the middle of the clock train. Shift registers SR09 and SR10 are cleared by the SYNC pulse in cyan. Error outputs for "TOO FEW", "TOO MANY" and "NO SYNC" are indicated in orange.

CLK pulse	Time (ns)	Shift Register	Bit Set	Event
1	6.5	SR09	7	
2	8.5	SR09	6	
3	10.5	SR09	5	Start of <i>CLR2</i>
4	12.5	SR09	4	
5	14.5	SR09	3	End of <i>CLR2</i>
6	16.5	SR09	2	
7	18.5	SR09	1	
8	20.5	SR09	0	S16 jumper for <i>STR</i>
9	22.5	SR10	7	S18 jumper for <i>STR</i>
10	24.5	SR10	6	S20 jumper for <i>STR</i>
11	26.5	SR10	5	S22 jumper for <i>STR</i>
12	28.5	SR10	4	S24 jumper for <i>STR</i> TOO FEW latch (DL73) reset
13	30.5	SR10	3	TOO MANY Error
14	32.5	SR10	2	
15	34.5	SR10	1	
16	36.5	SR10	0	NO SYNC Error

Table 6.6: The LTD synchronization signal timing from the shift registers SR09 and SR10 (see figure 6.7). *CLK* pulse refers to the number of pulses into the gated clock train. Time is measured from when the rising edge of *STR* arrives at the input latches (which defines the start of the beam pulse). Bit set refers to the shift register bit set by the clock pulse. Note the numbering goes from 7 down to 0. This is because the shift registers are set to shift left rather than right. At each clock pulse, the significant event, if any, is listed.

different error conditions: TOO FEW clock pulses, TOO MANY clock pulses and NO SYNC. Note that the condition of no clock pulses is not included here, but if there are no clock pulses, there will be no data coming from the LTDs.

Shift registers SR09 and SR10 in figure 6.7 basically count the number of clock pulses in the clock train and generate the appropriate synchronization pulses during the beam pulse. Bit 4 of the SR10 (the 12th clock pulse, see table 6.7) is connected to jumper S24 and to the reset of latch DL73 (see figure 6.7). The clock input of DL73 is connected to the *CLK* line. If there is at least one pulse in the clock train, it will set DL73. This latch is only reset if there are at least 12 clock pulses. So if DL73 is still set at the time *SYNC* comes, that means there were less than 12 clock pulses. This condition is checked with the AND gate AN14. The inputs for this AND gate are the output of DL73 and the *SYNC* pulse. The output of AN14 is the TOO FEW error signal. Bit 3 of SR10 (the 13th clock pulse) is the TOO MANY error signal. If there are more than 12 clock pulses, then bit 3 will be set. Bit 0 of SR10 (16th clock pulse) is the NO SYNC error signal.

Once an error signal is generated, it performs three functions as shown in figure 6.8. First, it flashes a LED on the LTD front panel (see figure 6.11). Second, it turns on a second LED on the front panel which is only turned off by the ERROR RESET button. Third, it generates an output pulse which can be sent to a scaler or to another LTD board. Each of these functions will be discussed in turn.

The bottom of the LTD front panel has three red LEDs, a red button and three more red LEDs as shown in figure 6.11. The bottom three LEDs are called the real time error lights. The top LED of the three (just below the button) is the NO SYNC error light. It is connected to the bit 0 of SR10 (the 16th clock pulse) as shown in figure 6.7. The output of this bit goes to OR13 and the output of OR13 is the NO SYNC error signal. The  $\overline{Q}$  (inverse) output of OR13 goes to the branch driver gate BD11 which is connected to the front panel LED. A branch driver is an ECL gate which produces a logic low output which only requires  $25\Omega$  impedance and which has a voltage level around -2V, compared to the nominal ECL level of -1.7V. Basically, this gate was designed to drive a LED since most LEDs operate at voltages in the range of -1.8V to -2.0V. The NO SYNC signal also sets the latching NO SYNC LED and goes to the error oscillator as will be discussed below.

The TOO MANY and TOO FEW error signals (see figure 6.7) are both connected to the clock inputs of two latches (see figure 6.8). In the case of TOO MANY these are latches DL61 and DL50 and for TOO FEW these are latches DL60 and DL51. The latches DL61 and DL60 generate the real time LED outputs. The *Q* output of each is connected to its own reset line by way of an RC circuit. Basically, these latches turn themselves off some fixed time after being set. The RC time constant is  $(50\Omega)(680\mu F) = 34 \text{ ms}$ . The  $\overline{Q}$  of these latches are connected to the inputs of the branch drivers BD13 and BD12 respectively. The outputs of the branch drivers are connected to the real time LEDs TOO MANY and TOO FEW on the front panel.

The error signals TOO MANY, TOO FEW and NO SYNC all go to the latching LEDs on the LTD front panel. These are the three red LEDs over the ERROR RESET button (see figure 6.11). When an error occurs, the corresponding latching LED comes on and stays on till the ERROR RESET button is pressed. The reason for this is to catch intermittent errors that may occur when the user is not looking at the real time error lights. Imagine that there is a brief problem with the

KGB module (a loose cable, a flakey DIP switch, etc.) so that all the LTD modules get clock trains with less than 12 pulses for a short period of time. As will be discussed below, the LTDs output an error signal which will be connected to scaler channels, so intermittent errors like this would be recorded in the data stream. But the error signals only indicate that an error occurred, not the nature of the error. However, the user could look at the LTD front panel and see that the TOO FEW latched LEDs were on and so determine the nature of the problem. So the latching error LEDs are a diagnostic tool for intermittent errors.

The circuit for the latching error lights is fairly simple. An error signal sets a latch. The  $\overline{Q}$  output of the latch goes to a branch driver which is connected to the front panel LED. The reset line of the latch is connected to ground through the ERROR RESET button. When the button is pressed, the reset line is shorted to ground, which is above the normal ECL logic high voltage level of -0.9V, and so the latch is reset. Looking at figure 6.8, the TOO MANY error signal is connected to DL50, the TOO FEW error signal is connected to DL51 and the NO SYNC error signal is connected to DL53. These are connected to the branch drivers BD14, BD15 and BD16 respectively.

There is an additional latch in figure 6.8 whose output is connected to the ERROR RESET lines (going to the resets of DL50, DL51 and DL53). This latch, DL52, is the power up reset. When the LTD module is first powered on, it is possible that false error signals may be generated. This could be due to changing voltage levels on the board as the voltage is first switched on or maybe because the LTD powers up in the middle of a clock train. Whatever the reason, false error signals would set the front panel latching error lights. Since it would be bothersome to press the ERROR RESET button on all the LTD modules every time a crate is powered up, the LTDs have an automatic power up reset for these LEDs.

The power up reset relies on two RC circuits. The clock input of DL52 is connected to one RC circuit with a time constant of about 2 s. Basically the voltage level on this input ramps up from -5V to 0V and will cross -1.3V (the ECL transition voltage) shortly after the power to the module is turned on. The latch will see this as a positive transition and so set the latch. The output of this latch is connected to the error reset line so it resets DL50, DL51 and DL53 thus turning off the latched error LEDs. The output of DL52 is also connected to its own reset line through a second RC circuit with a time constant around 30 ms. Therefore the latch will reset itself shortly after it is set. The power up reset latch will only go through this cycle once after the power is first turned on. If any of the latching error LEDs are accidentally set during power up, this circuit will reset them within a couple seconds.

In figure 6.8, all three error signals (TOO MANY, TOO FEW and NO SYNC) all input to the OR gate OR12. In addition, an external signal called ERROR INPUT also goes to OR12. The purpose of this will be explained below. The output of OR12 goes to the latch DL63 and the OR gate OR10 in figure 6.8. These gates are part of the error oscillator circuit of the LTD. Basically, this circuit generates an error output signal whenever there is an error of any sort on the LTD module. The output goes to the LTD front panel where it can be connected to a scaler channel. This scaler could then be read out every macro pulse along with the scaler channels connected to the LTD output bits. The purpose of the oscillator is to provide a signal of constant rate in the event of a continuous error. Imagine that an error occurs with the KGB (see chapter 4) such that there are more than 12 clock pulses in each clock train. In this case, the TOO MANY error signal

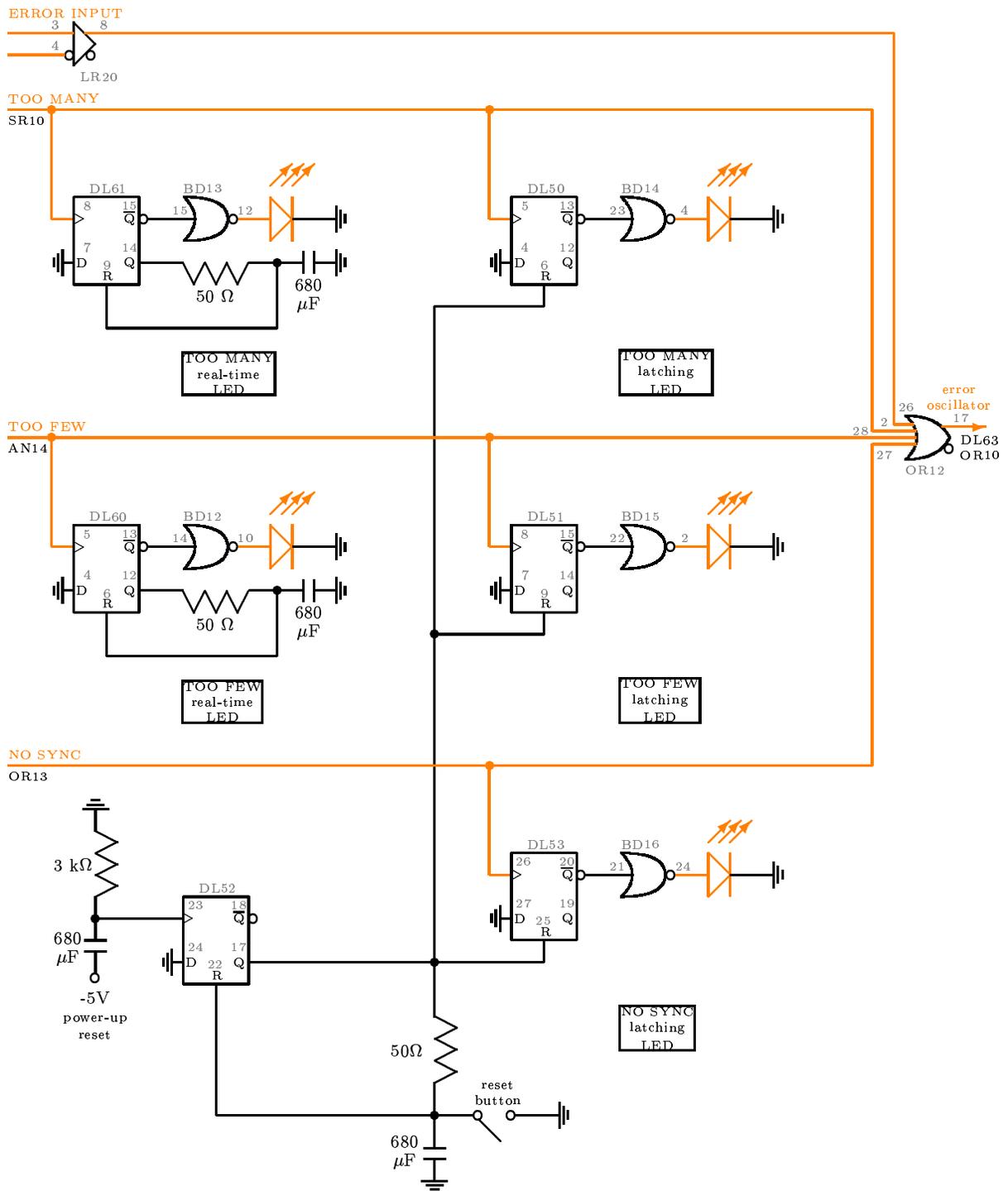


Figure 6.12: Block diagram for LTD error lights and outputs.

would be generated for every micro pulse (32 ns) so the rate of this signal would be 31.25 MHz. As it turns out, the Grenoble scalers used by the  $G^0$  experiment can handle this rate (see chapter 12) but other commercially available scalers cannot. For this reason, the error oscillator produces a maximum output rate that is more like 2 MHz which is fine for most scalers available. In the case of intermittent errors, the oscillator produces one pulse at the time of the error signal, then shuts off. So the output signal rate is equal to the error signal rate up to a maximum of about 2 MHz, after which it becomes constant at this value.

The heart of the error oscillator is a comparator (line receiver LR23 in figure 6.8) with a voltage divider on one side and a RC circuit on the other. A comparator has two inputs, a plus side (+) and a minus side (-). The output of the comparator depends on the relative voltage levels of the inputs. Basically the comparator takes the difference of the plus and minus sides. When this difference crosses zero volts going positive, the output goes to a logic high (-0.9V in ECL). When this difference crosses zero volts going negative, the output goes to logic low (-1.7V in ECL).

The latch DL63 in the error oscillator circuit acts as a switch to turn the oscillator circuit off and on. When DL63 is not set, its  $\overline{Q}$  output is at ECL high (-1.7V). This means that the  $\overline{Q}$  output of OR11 will always be at ECL low (-0.9V) and so the voltage levels on the plus and minus sides of the comparator (LR23) will not be changing. When DL63 is set, its  $\overline{Q}$  output will be at ECL low. Therefore the  $\overline{Q}$  output of OR11 will be determined by the  $\overline{Q}$  output of the comparator. Also, the plus and minus inputs of the comparator will be determined by the  $\overline{Q}$  output of OR11. Since the  $\overline{Q}$  output of OR11 is always inverted from the  $\overline{Q}$  output of the comparator, the circuit will oscillate. Figure 6.8 shows how the voltage levels change on the plus and minus sides of the comparator when the oscillator is running.

When there are no errors, the output of OR12 is ECL low (-1.7V) and the output of OR10 is also ECL low. Therefore the data and clock inputs of DL63 are both low and the  $\overline{Q}$  output of this latch is at ECL high (-0.9V). This output goes to OR11 and the  $\overline{Q}$  of this gate is connected to both sides of LR23 which acts as the comparator. The output of OR11 will initially be ECL low. There is an RC circuit on the minus side of the comparator and a voltage divider on the plus side. The voltage divider reduces the voltage level of the  $\overline{Q}$  output of OR11 slightly. So if the output is -1.7V, the plus side of the comparator will see -1.5V and if the output is -0.9V, it will see -1.1V. Initially, the plus side of the comparator will be at -1.5V and the minus side will be at -1.7V, so the  $\overline{Q}$  output of LR23 will be ECL low, -1.7V.

Figure 6.8 is a timing diagram for the error oscillator in figure 6.8 in the case when there is an error in just one clock train. When the error signal comes from OR12, DL63 will be set and the  $\overline{Q}$  output will drop to ECL low causing the  $\overline{Q}$  of OR11 to go to ECL high. On the plus side of the comparator, the voltage will change immediately to -1.1V. On the minus side, the RC circuit will cause the voltage level to rise with a time constant of  $(25\Omega)(0.1\mu F) = 2.5\mu s$ . It will approach -0.9V asymptotically and eventually cross -1.1V. At this point the  $\overline{Q}$  output of the comparator will go to ECL high. This is a positive transition and so will cause DL63 to clock in the level on its data input. In this case, since the error was only for one clock train, the output of OR12 is now low so DL63 clocks in a logic low causing its  $\overline{Q}$  output to go high. This, in turn, causes the  $\overline{Q}$  output of OR11 to go low. Now the plus side of the comparator goes to -1.5V and the minus side begins approaching -1.7V asymptotically. When the minus side crosses -1.5V, the  $\overline{Q}$  output of the comparator drops to ECL low. At this point, the oscillator is back to its original state. Effectively,

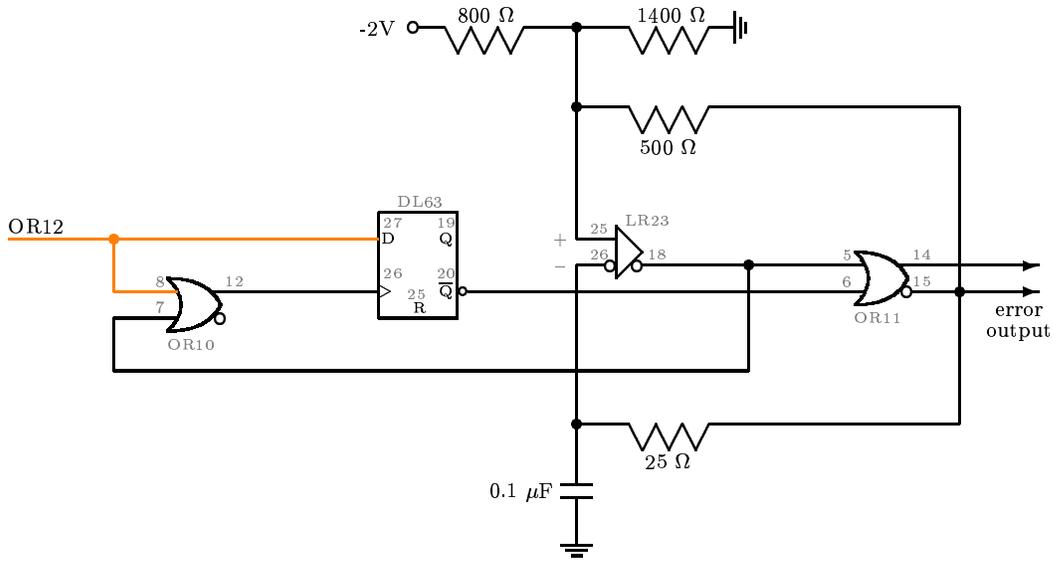


Figure 6.13: Block diagram for LTD error signal oscillator.

the oscillator makes one pulse, then shuts off.

Figure 6.8 is the timing diagram for the error oscillator in the case where there is a continuous error. So, for instance, when there is a problem with all, or nearly all the clock trains. The major difference here is that the data input of DL63 is always at ECL high, so every time the  $\overline{Q}$  output of LR23 goes high, DL63 clocks in a logic high and thus it remains set all the time. In this case, as described above, the output of the comparator will oscillate continuously. Once the error condition is fixed, the data input of DL63 will drop low and the oscillator will shut off.

## 6.9 Inputs and Outputs

Table 6.9 lists all the inputs and pin configurations for the LTD module while figure 6.11 shows the position of the input connectors on the LTD front panel. The power inputs (GND, -2V and -5V) are all in one connector called the POWER HEADER located on the back of the board. This connector plugs into the back plane of the LTD crate. All the other inputs are located on the LTD front panel. The front and back detector inputs are connected by a 10 pin DIN connector called DATA INPUTS at the top of the front panel. In the middle of the front panel are two twinaxial input connectors for *CLK* and *SYNC*. Just below this are three, two pin, Molex connectors. The top Molex connector is a copy of the *CLK* and is intended to be a handy reference for checking the *CLK* with an oscilloscope. The second Molex connector is the error signal output and the third Molex connector is the error signal input. Below the Molex connectors are three LEDs, a button and three more LEDs. This button is the ERROR RESET. Behind the button, on the LTD board itself, is another Molex connector which is connected to the button. The idea is that the error reset of two or more LTD modules may be linked through this connector. That way, when the ERROR

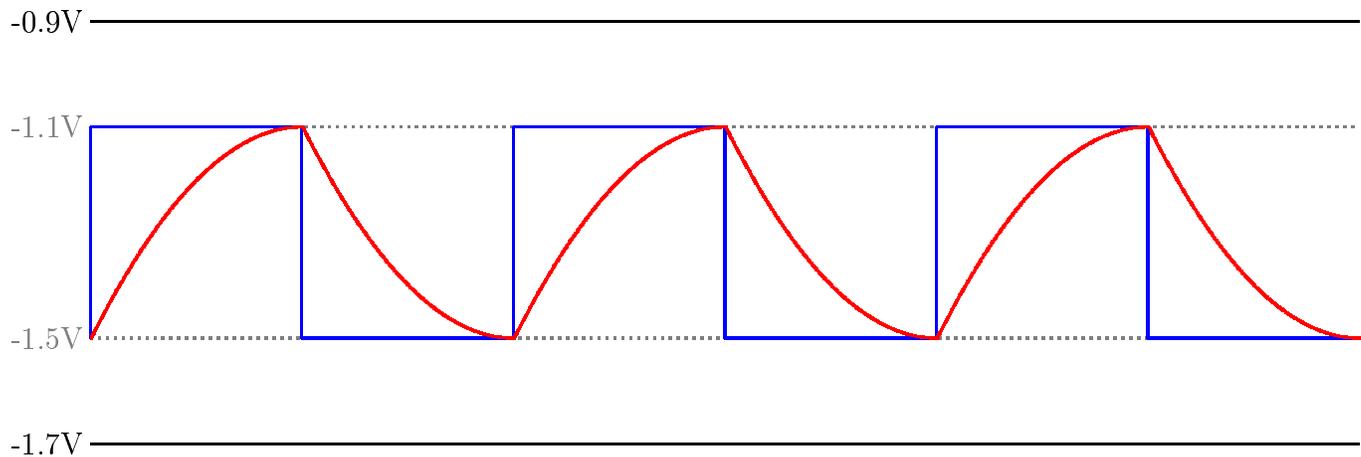


Figure 6.14: The voltage level versus time for both sides of the comparator in the oscillator of the error signal generator (figure 6.8). The blue square wave represents the voltage on the plus side of LR23 (pin 25) and the red line represents the voltage on the minus side (pin 26). The plus side is connected to a voltage divider so that its levels are either -1.1V or -1.5V which are slightly lower or higher than the true ECL voltage levels of -0.9V and -1.7V. The minus side of the comparator is connected to a RC circuit with its minimum and maximum voltage levels equal to normal ECL voltages. The comparator output will flip whenever the minus side voltage equals the plus side voltage.

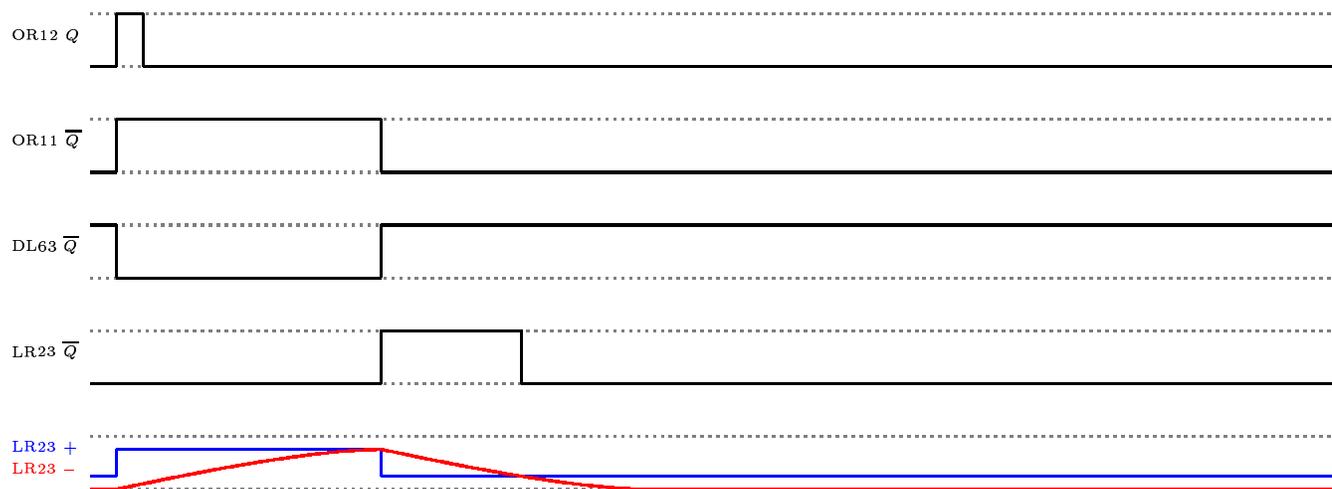


Figure 6.15: Timing diagram for the error oscillator (figure 6.8) in the case where there is an error in just one beam pulse. The dashed gray lines refer to the normal ECL levels of -1.7V and -0.9V. The blue and red curves show the voltage levels on the + and - sides of the comparator respectively.

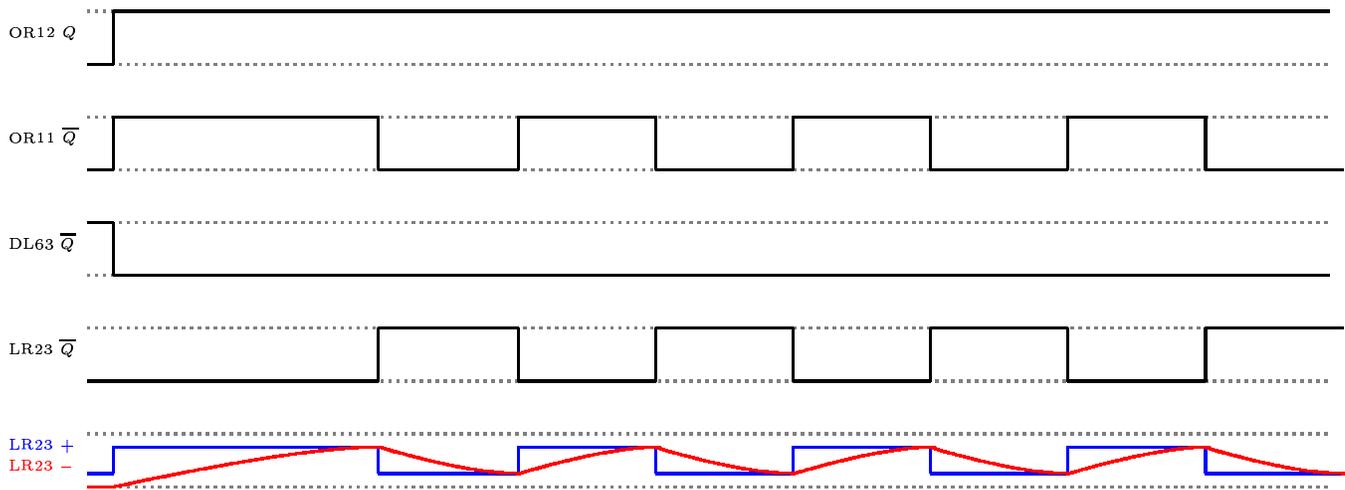


Figure 6.16: Timing diagram for the error oscillator (figure 6.8) in the case where there is a continuous error condition. The dashed gray lines refer to the normal ECL levels of -1.7V and -0.9V. The blue and red curves show the voltage levels on the + and - sides of the comparator respectively.

RESET button is pressed on one module, all the modules are reset.

Input	Connector	pins
CLK	CLK	twinaxial
SYNC	SYNC	twinaxial
ERROR IN	ERROR IN	twisted pair
RESET BUS	RESET BUS	twisted pair
Back top	SIGNAL INPUT	10,9
Back bottom	SIGNAL INPUT	8,7
Front top	SIGNAL INPUT	4,3
Front bottom	SIGNAL INPUT	2,1
power GND	POWER HEADER	2,4,6,8,10,12,14,16,18,20
power -5V	POWER HEADER	1,3,5,7,9
power -2V	POWER HEADER	11,13,15,17,19

Table 6.7: Inputs for the LTD board.

The LTD module has two basic groups of outputs which are the time digitization signals (see section 6.6) and the Buddy outputs (see section 6.4). The time digitization signals are output on two 50 pin female DIN connectors on the back of the module, one connector for each LTD channel. The individual bits are listed in table 6.9. These DIN connectors plug into male DIN connectors on the back plane of the LTD crate which in turn are connected to the Munger boards (see chapter 7) and eventually to scaler channels. The Buddy outputs go to a 10 pin DIN connector on the LTD front panel, just below the DATA INPUTS. Again, the pin configuration is listed in table 6.9. The error output signal is mentioned in the paragraph above.

Output	Connector	pins
CLK REFERENCE	CLK REFERENCE	twisted pair
ERROR OUT	ERROR OUT	twisted pair
“previous pulse” bottom	DEADTIME OUTPUT	2,1 (DT1)
“this pulse” bottom	DEADTIME OUTPUT	4,3 (DT2)
“previous pulse” top	DEADTIME OUTPUT	6,5 (DT3)
“this pulse” top	DEADTIME OUTPUT	8,7 (DT4)
bit 2	OUTPUT HEADER	1,2
bit 4	OUTPUT HEADER	3,4
bit 6	OUTPUT HEADER	5,6
bit 8	OUTPUT HEADER	7,8
bit 10	OUTPUT HEADER	9,10
bit 12	OUTPUT HEADER	11,12
bit 14	OUTPUT HEADER	13,14
bit 16	OUTPUT HEADER	15,16
bit 18	OUTPUT HEADER	17,18
bit 20	OUTPUT HEADER	19,20
bit 22	OUTPUT HEADER	21,22
bit 24	OUTPUT HEADER	23,24
bit 1	OUTPUT HEADER	25,26
bit 3	OUTPUT HEADER	27,28
bit 5	OUTPUT HEADER	29,30
bit 7	OUTPUT HEADER	31,32
bit 9	OUTPUT HEADER	33,34
bit 11	OUTPUT HEADER	35,36
bit 13	OUTPUT HEADER	37,38
bit 15	OUTPUT HEADER	39,40
bit 17	OUTPUT HEADER	41,42
bit 19	OUTPUT HEADER	43,44
bit 21	OUTPUT HEADER	45,46
bit 23	OUTPUT HEADER	47,48

Table 6.8: Outputs for the LTD board. Note, the bits and pin number for #OUTPUT HEADER (bottom channel) are identical to those of OUTPUT HEADER (top channel).

Name	Function
S16 - S24	Sets the time of <i>STR</i> and <i>CLR1</i> relative to <i>CLK</i> .
C1 - C4	Delays <i>CLR1</i> relative to <i>STR</i> .
BCK BUSY	Connects the back busy line to the input, top channel.
#BCK BUSY	Connects the back busy line to the input, bottom channel.
BCK GND	Selects back detector or GND for latch DATA input, top channel
#BCK GND	Selects back detector or GND for latch DATA input, bottom channel
STR NPN	Selects STR or NPN for the latch RESET, top channel.
#STR NPN	Selects STR or NPN for the latch RESET, bottom channel.
CLR1 DELAY	Adds 2ns to <i>CLR1</i> when using programmable delay chips.
STR DELAY	Adds 2ns to <i>STR</i> when using programmable delay chips.
SYNC CLK	Selects <i>CLK</i> or <i>CLK</i> for the sychronization shift registers.
TERMINATE	Terminates the line not used by SYNC CLK.

Table 6.9: List of jumpers on the LTD. Not included in this list are a series of jumpers that were never implemented. These jumpers were to be used to route the *CLK* lines to the shift registers through programmable delay chips, but these chips were not installed. A map of these jumpers is included on the silkscreen of the LTD boards.

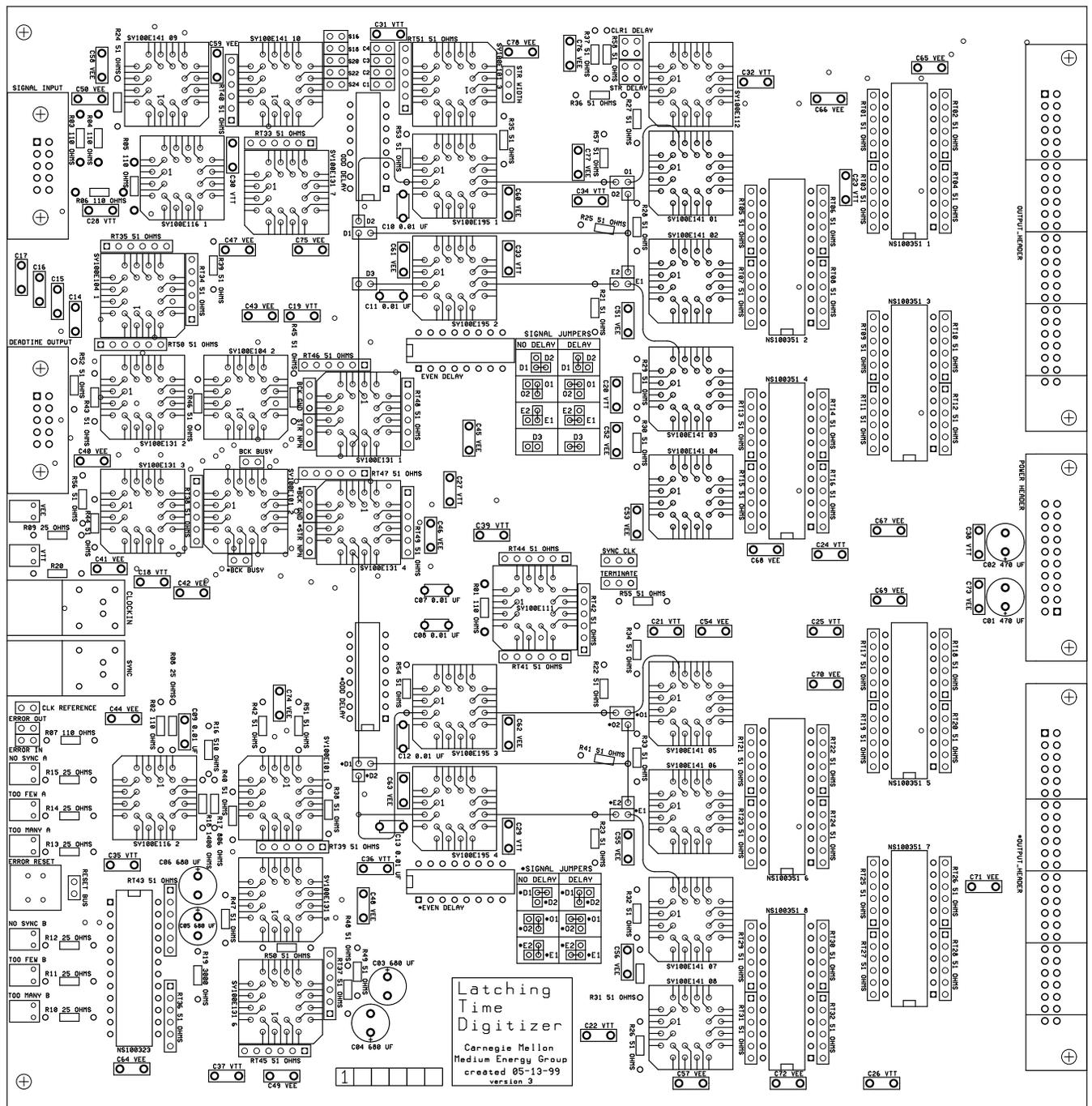
## 6.10 Jumpers and Switches

The LTD module has several different jumpers which allow it to be configured several different ways. All the jumpers are listed in table 6.10 along with their basic function. Most of the jumpers select various timing options while the rest select dead time configurations. Note, the timing option jumpers are in common to both LTD channels, so there is only one of each. For the rest, there is one set of jumpers for each of the two LTD channels. The naming convention is the the bottom channel has a # sign in front of the jumper label while the top channel does not. In the text below, only the jumper on the top channel is referenced, but the description is accurate for the jumpers on both channels.

Normally the LTD requires both the front and back detector signals, only the latch only sets when there is a coincidence between the two. However, for testing purposes, it is often easier to supply just one detector signal (the front detector since this sets the timing). In this case, the jumper BCK GND allows a user to switch the LTD to single detector mode. The jumper is located near chip DL1 (DL4 for the bottom channel, see figure 6.2 and table 6.3). If the jumper is on the upper two pins (near the BCK label), the LTD channel will be in single detector mode. If it is on the lower two pins, the LTD channel will require a coincidence of the front and back detectors.

## 6.11 Module Construction

Figure 6.17 shows the layout of the LTD six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. The LTD front panel is shown in figure 6.11. A parts list for the LTD module is given in table 6.11.



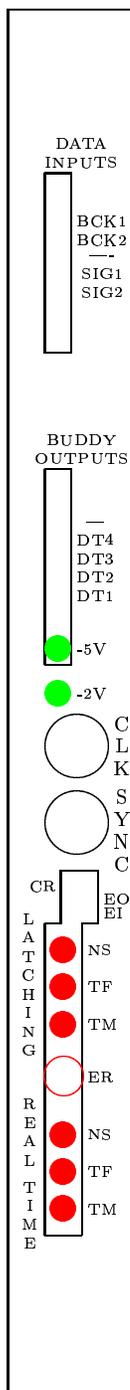


Figure 6.18: Front panel layout for the LTD module. The following abbreviations are used: TF=TOO FEW, TM=TOO MANY, NS=NO SYNC, CR=clk ref, EI=error in, EO=error out and ER=error reset.

Quan.	Description	Manufacturer	Part Number
62	0.1 $\mu$ F ceramic capacitor	Panasonic	ECK-F1E104ZV
2	470 $\mu$ F electrolytic capacitor	Panasonic	ECE-A1AU471
4	680 $\mu$ F electrolytic capacitor	Panasonic	EEU-FA1A681L
6	0.01 $\mu$ F ceramic capacitor	KEMET	CK05BX103K
39	51.1 $\Omega$ resistor	Yageo	MFR-25FBB-51R1
8	24.9 $\Omega$ resistor	Yageo	MFR-25FBB-24R9
7	110 $\Omega$ resistor	Yageo	MFR-25FBB-110R
1	511 $\Omega$ resistor	Yageo	MFR-25FBB-511R
1	806 $\Omega$ resistor	Yageo	MFR-25FBB-806R
1	1400 $\Omega$ resistor	Yageo	MFR-25FBB-1K40
1	3010 $\Omega$ resistor	Yageo	MFR-25FBB-3K01
51	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
3	Quad 4-Input OR Gate	Micrel	SY100E101JC
2	Quad 2-Input AND Gate	Micrel	SY100E104JC
1	1:9 Differential Clock Driver	Micrel	SY100E111JC
1	Quad Driver	Micrel	SY100E112JC
2	Quad Differential Line Receiver	Micrel	SY100E116JC
7	4-Bit D Flip-Flop	Micrel	SY100E131JC
10	8-Bit Shift Register	Micrel	SY100E141JC
8	Hex D Registers	Fairchild	100351DC
1	Hex Bus Driver	Fairchild	100323PC
6	red LED	Chicago Miniature	5300H1LC
1	green LED	Chicago Miniature	5300H5LC
4	8 position DIP switch	CTS corp.	208-8
1	push button switch red cap	Cutler-Hammer	B8600 P281R
30	28 pin PLCC socket	FCI	PLCC-28-P-T
2	10 pin RA male DIN con.	FCI	71922-110
2	10 pin female DIN con.	FCI	71602-010
1	20 pin RA socket DIN con.	Hirose	PCN13-20S-2.54DS
2	50 pin RA socket DIN con.	Hirose	PCN13-50S-2.54DS
2	twinaxial receptacle	Lemo	EPL.0S.302.HLN
3	dual row header, right angle	Sullins Electronics	PTC36DBAN
14	dual row header	Sullins Electronics	PTC36DAAN
25	single row header	Sullins Electronics	PTC36SAAN

Table 6.10: Parts List for the LTD board.

## 6.12 Deadtime Corrections

Definitions of dead time variables:

$$\begin{aligned}
 R_n &= \text{True rate in the } n\text{th bin.} \\
 r_n &= \text{Observed rate in the } n\text{th bin.} \\
 \tau_n &= \text{width of the } n\text{th bin.} \\
 R_n \tau_n &= \text{average number of hits in } n\text{th bin.}
 \end{aligned}$$

Average number of hits in one micro pulse:

$$\sum_{i=0}^{24} R_i \tau_i \tag{6.4}$$

Probability of no hit in the previous micro pulse:

$$e^{-\sum_{i=0}^{24} R_i \tau_i} \tag{6.5}$$

Observed rate in the  $n$ th bin of a non-vetoed clock train:

$$r_n e^{+\sum_{i=0}^{24} R_i \tau_i} \tag{6.6}$$

Average number of observed hits before the  $n$ th bin (in one non-vetoed clock train), the probability of a hit in the preceding  $n$ th bin:

$$\sum_{j=0}^{n-1} r_j \tau_j e^{+\sum_{i=0}^{24} R_i \tau_i} \tag{6.7}$$

Probability of no hit in the preceding  $n$ th bin:

$$1 - \sum_{j=0}^{n-1} r_j \tau_j e^{+\sum_{i=0}^{24} R_i \tau_i} \tag{6.8}$$

Probability of no hit in  $n$ th bin:

$$e^{-R_n \tau_n} \tag{6.9}$$

Probability of a seeing a hit in the  $n$ th bin:

$$1 - e^{-R_n \tau_n} \tag{6.10}$$

The probability of having a non-vetoed hit in the  $n$ th bin is the product of equations 6.5, 6.8 and 6.10:

$$(e^{-\sum_{i=0}^{24} R_i \tau_i}) \left(1 - \sum_{j=0}^{n-1} r_j \tau_j e^{+\sum_{i=0}^{24} R_i \tau_i}\right) (1 - e^{-R_i \tau_i}) \quad (6.11)$$

Observed rate in the  $n$ th bin (the GOD equation):

$$r_n = \frac{1}{\tau_n} \left( e^{-\sum_{i=0}^{24} R_i \tau_i} - \sum_{j=0}^{n-1} r_j \tau_j \right) (1 - e^{-R_i \tau_i}) \quad (6.12)$$

# Chapter 7

## Munger

### 7.1 Function

The LTD boards (see chapter 6) have 24 pairs of differential ECL outputs per channel which correspond to 24 time bins, of which 23 are nominally 1 ns wide. There are a total of 64 detectors in the North American quadrants and thus 64 LTD channels. A total of 1536 scaler channels is required to monitor all the LTD time bins. The Grenoble scaler modules (see section 12.4) have 32 channels each, so a total of 48 such modules would be required. At present, the  $G^0$  collaboration has purchased enough scaler modules to cover all the time bins on all the LTD channels. Eventually it may not be necessary or desirable to measure the entire spectrum with 1 ns resolution. In that case, the munger module provides a mechanism for selecting only particular time bins to monitor.

The order of the 24 LTD time bits are shown in figure 6.9. Basically, they are in order of bit number, first even then odd. This arrangement makes it difficult to select any one particular bit to monitor with the scalers. It would be preferable if the outputs were grouped by bit number and ordered by LTD channel number. For instance, bit 1, LTD 1,2,3,4,5,6,7 and 8 then bit 2, LTD 1,2,3,4,5,6,7 and 8 and so forth. This is the purpose of the munger module. It takes the output bits from 8 different LTD channels and reorders them by bit number. In this way, a single scaler module can monitor a particular bit on 8 different LTDs channels at once, rather than monitoring all 24 bits from a single LTD channel. This makes it possible to select which bits are monitored and which are not.

### 7.2 Inputs and Outputs

The munger module is comprised of three sections, called mini-mungers. Each mini-munger takes 8 of the 24 bits from 8 LTD channels and produces 8 outputs.

### 7.3 Labels

### 7.4 Module Construction

Figure 7.1 shows the layout of the mini-munger four layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the munger

LTD	LTD bits mini-munger 1	LTD bits mini-munger 2	LTD bits mini-munger 3
1	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
2	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
3	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
4	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
5	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
6	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
7	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23
8	2,4,6,8,10,12,14,16	18,20,22,24,1,3,5,7	9,11,13,15,17,19,21,23

Table 7.1: .

	Output connector							
	1	2	3	4	5	6	7	8
mini-munger 1	bit 2 LTDs 1 to 8	bit 4 LTDs 1 to 8	bit 6 LTDs 1 to 8	bit 8 LTDs 1 to 8	bit 10 LTDs 1 to 8	bit 12 LTDs 1 to 8	bit 14 LTDs 1 to 8	bit 16 LTDs 1 to 8
mini-munger 2	bit 18 LTDs 1 to 8	bit 20 LTDs 1 to 8	bit 22 LTDs 1 to 8	bit 24 LTDs 1 to 8	bit 1 LTDs 1 to 8	bit 3 LTDs 1 to 8	bit 5 LTDs 1 to 8	bit 7 LTDs 1 to 8
mini-munger 3	bit 9 LTDs 1 to 8	bit 11 LTDs 1 to 8	bit 13 LTDs 1 to 8	bit 15 LTDs 1 to 8	bit 17 LTDs 1 to 8	bit 19 LTDs 1 to 8	bit 21 LTDs 1 to 8	bit 23 LTDs 1 to 8

Table 7.2: .

Output	Bits	Pins	Input	Pins	Output	Bits	Pins	Input	Pins
1	2,18, 9	1, 2	LTD 1	1, 2	5	10, 1,17	1, 2	LTD 1	9,10
1	2,18, 9	3, 4	LTD 2	1, 2	5	10, 1,17	3, 4	LTD 2	9,10
1	2,18, 9	5, 6	LTD 3	1, 2	5	10, 1,17	5, 6	LTD 3	9,10
1	2,18, 9	7, 8	LTD 4	1, 2	5	10, 1,17	7, 8	LTD 4	9,10
1	2,18, 9	9,10	LTD 5	1, 2	5	10, 1,17	9,10	LTD 5	9,10
1	2,18, 9	11,12	LTD 6	1, 2	5	10, 1,17	11,12	LTD 6	9,10
1	2,18, 9	13,14	LTD 7	1, 2	5	10, 1,17	13,14	LTD 7	9,10
1	2,18, 9	15,16	LTD 8	1, 2	5	10, 1,17	15,16	LTD 8	9,10
2	4,20,11	1, 2	LTD 1	3, 4	6	12, 3,19	1, 2	LTD 1	11,12
2	4,20,11	3, 4	LTD 2	3, 4	6	12, 3,19	3, 4	LTD 2	11,12
2	4,20,11	5, 6	LTD 3	3, 4	6	12, 3,19	5, 6	LTD 3	11,12
2	4,20,11	7, 8	LTD 4	3, 4	6	12, 3,19	7, 8	LTD 4	11,12
2	4,20,11	9,10	LTD 5	3, 4	6	12, 3,19	9,10	LTD 5	11,12
2	4,20,11	11,12	LTD 6	3, 4	6	12, 3,19	11,12	LTD 6	11,12
2	4,20,11	13,14	LTD 7	3, 4	6	12, 3,19	13,14	LTD 7	11,12
2	4,20,11	15,16	LTD 8	3, 4	6	12, 3,19	15,16	LTD 8	11,12
3	6,22,13	1, 2	LTD 1	5, 6	7	14, 5,21	1, 2	LTD 1	13,14
3	6,22,13	3, 4	LTD 2	5, 6	7	14, 5,21	3, 4	LTD 2	13,14
3	6,22,13	5, 6	LTD 3	5, 6	7	14, 5,21	5, 6	LTD 3	13,14
3	6,22,13	7, 8	LTD 4	5, 6	7	14, 5,21	7, 8	LTD 4	13,14
3	6,22,13	9,10	LTD 5	5, 6	7	14, 5,21	9,10	LTD 5	13,14
3	6,22,13	11,12	LTD 6	5, 6	7	14, 5,21	11,12	LTD 6	13,14
3	6,22,13	13,14	LTD 7	5, 6	7	14, 5,21	13,14	LTD 7	13,14
3	6,22,13	15,16	LTD 8	5, 6	7	14, 5,21	15,16	LTD 8	13,14
4	8,24,15	1, 2	LTD 1	7, 8	8	16, 7,23	1, 2	LTD 1	15,16
4	8,24,15	3, 4	LTD 2	7, 8	8	16, 7,23	3, 4	LTD 2	15,16
4	8,24,15	5, 6	LTD 3	7, 8	8	16, 7,23	5, 6	LTD 3	15,16
4	8,24,15	7, 8	LTD 4	7, 8	8	16, 7,23	7, 8	LTD 4	15,16
4	8,24,15	9,10	LTD 5	7, 8	8	16, 7,23	9,10	LTD 5	15,16
4	8,24,15	11,12	LTD 6	7, 8	8	16, 7,23	11,12	LTD 6	15,16
4	8,24,15	13,14	LTD 7	7, 8	8	16, 7,23	13,14	LTD 7	15,16
4	8,24,15	15,16	LTD 8	7, 8	8	16, 7,23	15,16	LTD 8	15,16

Table 7.3: Inputs and outputs for the mini-munger. Each mini-munger board reorders 8 bits from 8 LTD channels. Thus it takes 3 mini-munger boards to reorder all 24 bits from the 8 LTD channels. The first mini-munger handles bits 2,4,6,8,10,12,14 and 16. The second mini-munger handles bits 18,20,22,24,1,3,5 and 7. The third mini-munger handles bits 9,11,13,15,17,19,21 and 23. This is why three input connectors are listed in the Bits columns. The bits are labelled accordingly on each of the three mini-mungers in a single Munger unit.

Quan.	Description	Manufacturer	Part Number
16	16 pin male DIN con.	FCI	71918-116
16	16 pin female DIN con.	FCI	71602-316
4	dual row header	Sullins Electronics	PTC36DAAN

Table 7.4: Parts List for mini-munger board.

module is given in table 7.4.

Figure 7.1: Layout of the mini-munger board (MUNGER.BD1).

# Chapter 8

## CEBAF Board

### 8.1 Function

The function of the CEBAF board is to provide timing signals to the KGB (see Chapter 4) when the timing signals normally provided by the accelerator are not available. This should only be used for testing purposes since the signals it generates are in no way synchronized with the accelerator master clock or the beam pickoff.

The CEBAF board generates a 500Mhz clock signal to simulate the signal derived from the CEBAF master clock (Actually the 1497Mhz clock is divided down to a 499Mhz clock but it is nominally referred to as 500Mhz) and generates a simulation beam pickoff (Yo!) signal.

### 8.2 Inputs and Outputs

The CEBAF board has no front panel inputs. It requires power from the backplane as described in Appendix A.

The outputs of the CEBAF board are the simulated 500Mhz CLOCK and a divided down copy of CLOCK which has a period of 32ns called YO. YO simulates the beam pickoff signal from the accelerator. The CLOCK output is a female twinaxial connector which outputs an ECL signal. There are two different types of YO output. The first is a twinaxial connector which outputs an ECL signal and the second is a set of 8 twisted pair male connectors which output ECL signals. Both types of YO output are identical with respect to the signal.

The inputs and outputs of the CEBAF board are listed in Table 8.2 and Table 8.2.

### 8.3 Internal Settings

There are no internal settings on the CEBAF board.

Input	Connector	pins
CLOCK	CLOCK	twinaxial
YO	YO	twinaxial
power GND	POWER HEADER	2,4,6,8,10,12,14,16,18,20
power -5V	POWER HEADER	1,3,5,7,9
power -2V	POWER HEADER	11,13,15,17,19

Table 8.1: Inputs for the CEBAF board.

Output	Connector	pins
CLOCK	CLOCK	twinaxial
YO	YO	twinaxial
YO copy 1	YO OUTPUTS	1, 2
YO copy 2	YO OUTPUTS	3, 4
YO copy 3	YO OUTPUTS	5, 6
YO copy 4	YO OUTPUTS	7, 8
YO copy 5	YO OUTPUTS	9,10
YO copy 6	YO OUTPUTS	11,12
YO copy 7	YO OUTPUTS	13,14
YO copy 8	YO OUTPUTS	15,16

Table 8.2: Outputs for the CEBAF board.

## 8.4 Module Construction

Figure 8.1 shows the layout of the CEBAF six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the CEBAF module is given in table 8.4.

Figure 8.1: Layout of the CEBAF board (CEBAF.BD1).

Quan.	Description	Manufacturer	Part Number
2	28 pin PLCC socket	FCI	PLCC-28-P-T
2	twinaxial receptacle	Lemo	EPL.0S.302.HLN
1	1:9 Differential Clock Driver	Micrel	SY100E111JC
1	8-Bit Ripple Counter	Micrel	SY100E137JC
7	0.1 $\mu$ F ceramic capacitor	Panasonic	ECK-F1E104ZV
2	470 $\mu$ F electrolytic capacitor	Panasonic	ECE-A1AU471
4	51.1 $\Omega$ resistor	Yageo	MFR-25FBB-51R1
4	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
1	20 pin RA socket DIN con.	Hirose	PCN13-20S-2.54DS
1	20 pin RA plug DIN con.	Hirose	PCN10-20P-2.54DS
1	500 MHz ECL clock osc.	Vectron	CO-454C-OXF@500.0MHz

Table 8.3: Parts List for CEBAF

# Chapter 9

## Digitally Adjustable Divider and Delay Board (DADDY)

### 9.1 Function

### 9.2 Inputs and Outputs

### 9.3 Internal Settings

### 9.4 Module Construction

Figure 9.1 shows the layout of the DADDY six layer printed circuit board. The name and location of the OrCAD files for this board may be found in table D. A parts list for the DADDY module is given in table 9.4.

Input	Connector	pins
LEN	LEN	Lemo coaxial
CLK	CLK	Lemo coaxial
DATA	DATA	Lemo coaxial
signal	I/O	1,2
power GND	POWER HEADER	2,4,6,8,10,12,14,16,18,20
power -5V	POWER HEADER	1,3,5,7,9
power -2V	POWER HEADER	11,13,15,17,19

Table 9.1: Inputs for the DADDY board.

Input	Connector	pins
undelayed 0	UNDELAYED OUTPUT	19,20
undelayed 1	UNDELAYED OUTPUT	17,18
undelayed 2	UNDELAYED OUTPUT	15,16
undelayed 3	UNDELAYED OUTPUT	13,14
undelayed 4	UNDELAYED OUTPUT	11,12
undelayed 5	UNDELAYED OUTPUT	9,10
undelayed 6	UNDELAYED OUTPUT	7,8
undelayed 7	UNDELAYED OUTPUT	5,6
undelayed 8	I/O	3,4
delayed 0	DELAYED OUTPUT	19,20
delayed 1	DELAYED OUTPUT	17,18
delayed 2	DELAYED OUTPUT	15,16
delayed 3	DELAYED OUTPUT	13,14
delayed 4	DELAYED OUTPUT	11,12
delayed 5	DELAYED OUTPUT	9,10
delayed 6	DELAYED OUTPUT	7,8
delayed 7	DELAYED OUTPUT	5,6
delayed 8	I/O	5,6

Table 9.2: Outputs for the DADDY board.

Name	Function
RC	Sets the divisor of the ripple counter
SR	Sets the divisor of the shift registers
BYPASS/NO	Bypass ripple counter, or not
RC/NO RC	Bypass ripple counter, or not
SR/NO SR	Bypass shift registers, or not
#SR/#NO SR	Bypass shift registers, or not

Table 9.3: List of jumpers on the DADDY board.

Figure 9.1: Layout of the DADDY board (DADDY.BD1).

Quan.	Description	Manufacturer	Part Number
57	0.1 $\mu$ F ceramic capacitor	Panasonic	ECK-F1E104ZV
2	470 $\mu$ F electrolytic capacitor	Panasonic	ECE-A1AU471
3	coaxial receptacle	Lemo	EPL.00.250.NTN
14	51.1 $\Omega$ resistor	Yageo	MFR-25FBB-51R1
1	110 $\Omega$ resistor	Yageo	MFR-25FBB-110R
3	511 $\Omega$ resistor	Yageo	MFR-25FBB-511R
3	24.9 $\Omega$ resistor	Yageo	MFR-25FBB-24R9
38	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
3	Quad 2-Input AND Gate	Micrel	SY100E104JC
2	1:9 Differential Clock Driver	Micrel	SY100E111JC
3	Quad Driver	Micrel	SY100E112JC
1	Quad Differential Line Receiver	Micrel	SY100E116JC
2	4-Bit D Flip-Flop	Micrel	SY100E131JC
2	8-Bit Ripple Counter	Micrel	SY100E137JC
2	8-Bit Shift Register	Micrel	SY100E141JC
16	Programmable Delay Chip	Micrel	SY100E195JC
3	8-Bit Shift Register	Fairchild	100341PC
31	28 pin PLCC socket	FCI	PLCC-28-P-T
1	20 pin RA socket DIN con.	Hirose	PCN13-20S-2.54DS
2	20 pin RA plug DIN con.	Hirose	PCN10-20P-2.54DSA
1	10 pin RA male DIN con.	FCI	71922-110
32	dual row header	Sullins Electronics	PTC36DAAN
13	single row header	Sullins Electronics	PTC36SAAN
3	NPN bipolar transistor	NTE elec.	NTE108

Table 9.4: Parts List for the DADDY board.

# Chapter 10

## The Grey Noise Box and White Noise Fanout Module

### 10.1 Function

The function of the Grey Noise Box (GNB) is to provide a random signal for use in determining the widths of the LTD time bins (see chapter 6) and for studying the LTD dead time. The random signals are generated by a PMT viewing two LEDs through a mask with a small aperture. The PMT and LEDs are contained inside a light tight tube within the GNB (see figure 10.1). One LED is called the SOURCE LED and the other is called the BACKGROUND (BKG) LED, both have adjustable intensities.

The bin widths are determined by using one LED to generate a low rate, random signal which can be fanned out to multiple LTD channels. Since the time distribution of the random signals is flat, the measured number of counts in each LTD time bin will be proportional to the width of the bin. Using a low rate source ensures that dead time effects are negligible in determining the widths.

LTD dead time studies may be performed using both the SOURCE and BKG LEDs (see section 6.12). The idea is to vary the intensity of the BKG LED from 0 Hz to some large value (on the order of MHz) but hold the SOURCE LED at a fixed intensity. At each BKG intensity, data is collected while the SOURCE LED is repeatedly turned off and on. Dead time corrections are then applied to the (BKG+SOURCE) and BKG only samples. Subtraction of the former from the latter will be the dead time corrected rate of just the SOURCE LED alone. This corrected rate should be independent of the varying BKG rate. The GNB allows the intensity of both LEDs to be adjusted. It also has a TTL disable input for the SOURCE LED which allows it to be turned off and on under computer control.

Figure 10.1 shows a schematic of the GNB. An internal 5 VDC power supply produces power for the LEDs and front panel displays. For both the SOURCE and BKG LEDs, there is an external 1 k $\Omega$  potentiometer used to adjust the intensity and two internal 100 k $\Omega$  potentiometers used to set the minimum and maximum intensities. Basically these two internal pots keep the intensity values within a useful range. These were initially adjusted with a PMT voltage of 1850 V. There are two front panel displays (see figure 10.1) which display the voltage drop across a 110  $\Omega$  resistor in series with each LED. The voltage displayed is proportional to the intensity of the LED.

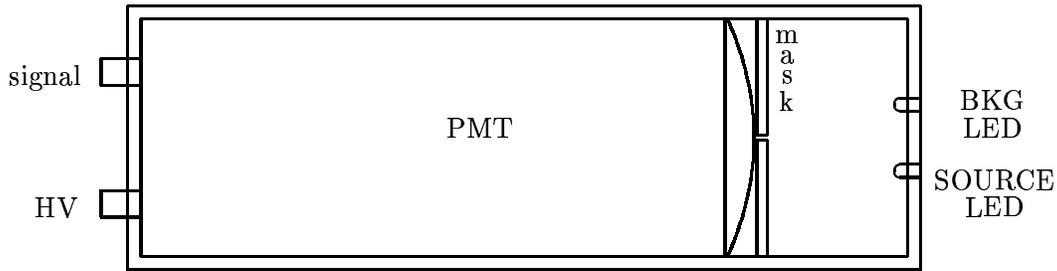


Figure 10.1: The PMT and LED configuration used to generate random signals within the GNB.

Component	Function
PMT HV	photomultiplier tube high voltage (1850 V) input
PMT signal	PMT signal output
TTL disable	TTL logic high input turns off SOURCE LED
SOURCE meter	measures voltage proportional to current draw of SOURCE LED
BKG meter	measures voltage proportional to current draw of BKG LED
Power switch	turns AC power on/off
BKG switch	turns BKG LED on/off
SOURCE adjust	varies voltage to SOURCE LED
BKG adjust	varies voltage to BKG LED

Table 10.1: Table of GNB front panel components.

## 10.2 Inputs, Outputs and Parts List

The inputs and outputs of the GNB are straight forward. Table 10.1 has a list of all inputs and outputs for the GNB while figure 10.1 shows the arrangement of the front panel. The GNB must be plugged into a standard 120 VAC three plug receptacle with the power cord at the rear of the box. The POWER switch near the center of the front panel turns on the internal 5 VDC supply. The LED next to this switch indicates when the power is on. The PMT HV is provided externally through a SHV connector, labelled PMT HV, on the front panel. The PMT signal is output through a BNC connector just above this. There are two black knobs, one on the SOURCE side (left) and one on the BACKGROUND side (right), which are used to vary the intensities of the SOURCE and BKG LEDs respectively. The two LCD displays show a voltage proportional to the current used by the LEDs. The SOURCE LED may be turned off using the TTL DISABLE connector. A TTL logic high signal input here will turn the SOURCE LED off, so the default is for the LED to be on. A switch on the far right side of the front panel is used to turn the BKG LED on or off. Table 10.2 lists all the parts used to construct the GNB.

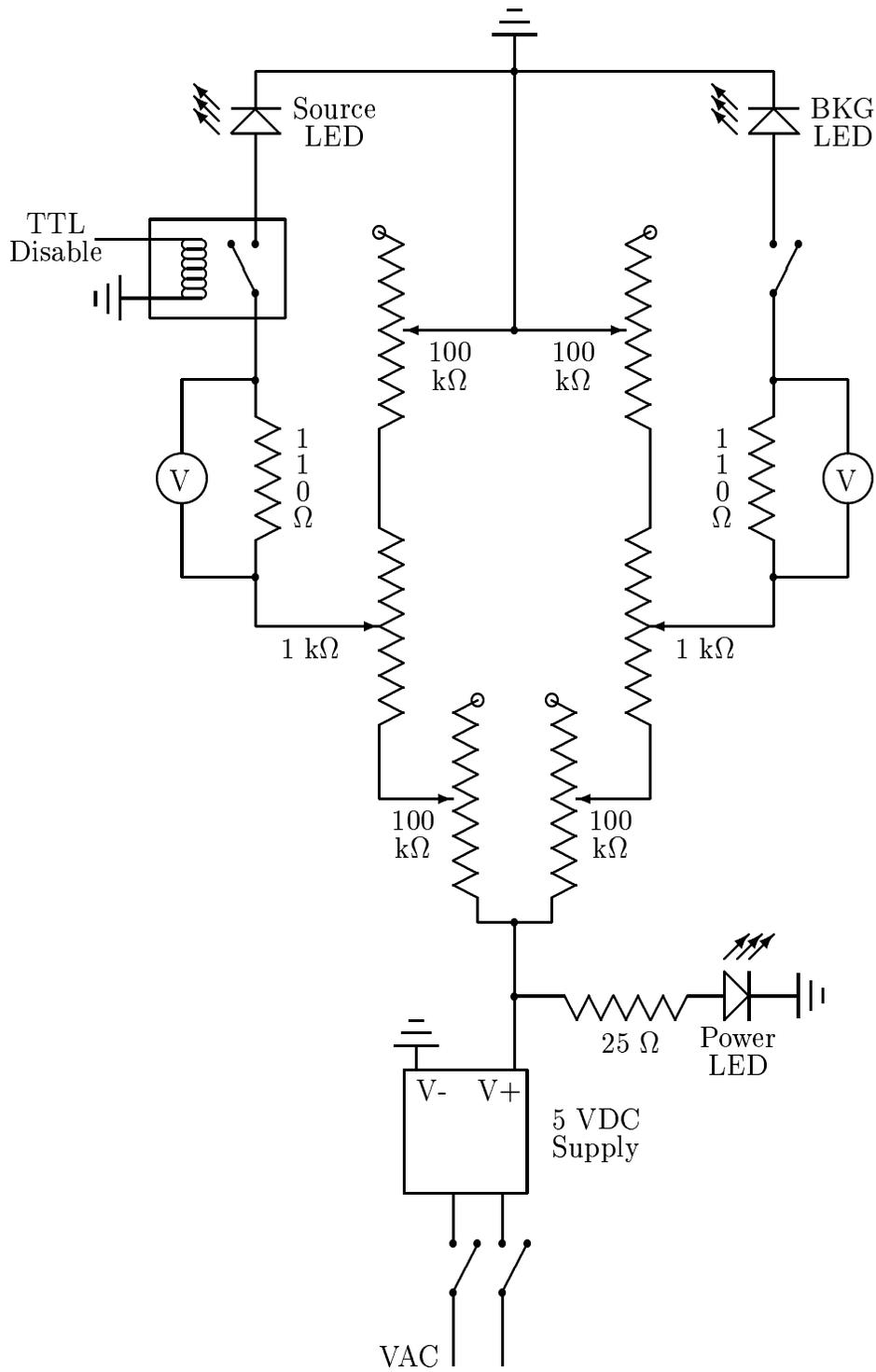


Figure 10.2: Schematic of the GNB.

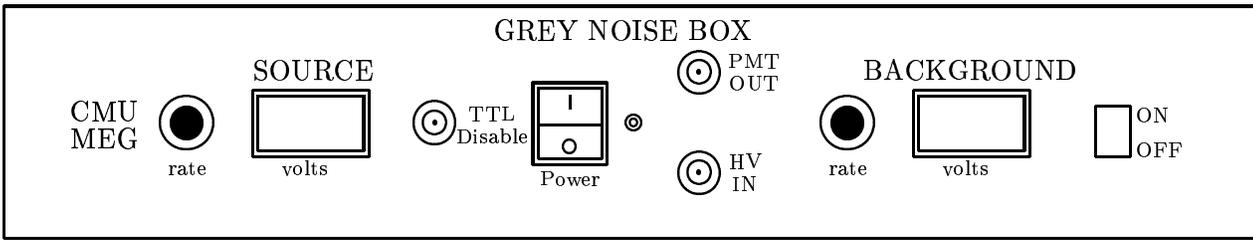


Figure 10.3: Front panel of the GNB.

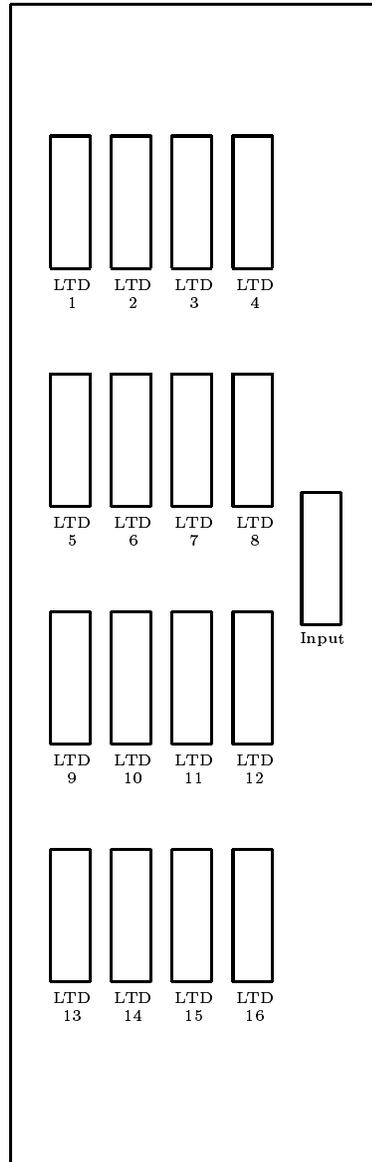


Figure 10.4: The front panel for the White Noise Fanout module.

Pins	Input	Output
1, 2	Backup	Backup 1
3, 4	—	Backup 2
5, 6	—	—
7, 8	Signal	Signal 1
9,10	—	Signal 2

Table 10.2: Table of WNF inputs and outputs. Note that only one output connector is shown here but all 16 are identical in function.

Quan.	Description	Manufacturer	Part Number
1	10X17X3 rack mount cabinet	Bud Indust.	AC-416
1	3 $\frac{1}{2}$ X19 front panel	Bud Indust.	PA-1132-MG
2	BNC bulkhead connector	Amphenol	31-220N-RFX
1	SHV bulkhead connector	Kings Elec.	1709-1
2	panel mount 1 k $\Omega$ pot.	Spectrol	534-1-1-102
2	pot. knob, black	Clarostat	DDS-50-2-5
3	LED green T-1 $\frac{3}{4}$	Chicago Lamp	CMD5453
1	panel mount rocker switch DPST	C&K/ITT/Cannon	C222J12S205PQF
1	panel mount rocker switch DPST	Carling Tech.	62115929-0-0-V
1	PCB mount DIP relay SPDT	Magnecraft	W172DIP-5
1	AC/DC PCB power supply	Cosel U.S.A.	YS1505A
2	panel mount voltmeter	Red Lion Cont.	MDMV0000
2	voltmeter cable assembly	Red Lion Cont.	HWK70000
2	1.0 K $\Omega$ Potentiometer	Bourns	3296W-1-102
2	100 K $\Omega$ Potentiometer	Bourns	3296W-1-104
2	110 $\Omega$ resistor	Yageo	MFR-25FBB-110R
1	24.9 $\Omega$ resistor	Yageo	MFR-25FBB-24R9

Table 10.3: Parts List for GNB.

Quan.	Description	Manufacturer	Part Number
1	NIM Double wide module	PMF	01-010R
1	NIM power connector male	PMF	202515-1
1	NIM power connector hood	PMF	202394-2
42	0.1 $\mu\text{F}$ ceramic capacitor	Panasonic	ECU-S1H104KBB
8	1.0 $\mu\text{F}$ tantalum capacitor	Panasonic	ECS-F1VE105K
2	26.1 $\Omega$ resistor	Yageo	MFR-25FBBF-26R1
6	51.1 $\Omega$ resistor	Yageo	MFR-25FBBF-51R1
2	82.5 $\Omega$ resistor	Yageo	MFR-25FBBF-82R5
2	88.7 $\Omega$ resistor	Yageo	MFR-25FBBF-88R7
2	150 $\Omega$ resistor	Yageo	MFR-25FBBF-150R
32	6 pin 51 $\Omega$ resistor network	CTS corp.	77061510
1	Quad Driver	Micrel	SY100E112JC
4	Negative Voltage Reg.	National Semiconductor	LM337T
8	Quad Driver	Fairchild	100313DC
17	10 Pin DIN con. w/flanges	3M	4610-6050

Table 10.4: Parts List for WNF.

# Chapter 11

## Integration

# Chapter 12

## Commercial Electronics

**12.1 Constant Fraction Discriminators (CFD)**

**12.2 FASTBUS ADCs**

**12.3 FASTBUS TDCs**

## 12.4 Grenoble 32-Bit Scalers

The Grenoble 32-Bit Scalers are VME Scaler modules designed by ISN Grenoble. They have the following characteristics:

- 32 differential ECL logical inputs, distributed on two 34 point connectors, with a possible selection of the active edge
- 32 bit counting
- A 140 Mega-Hertz maximum frequency value ( on 32 bits )
- Input for inhibition inputs ( INH )
- Input for counter value memorization (LO )
- Common Input for all the counters ( CI)
- Input for counter RESET ( RST )
- Input for the memorization of input states in an internal register ( PAT )
- VME addressing space in A24/D16 and A32/D32 modes
- Possibility of a local mode ( without VME ) with a local microcontroller
- RS232 Input/Output for the connection with a monitor for this local mode
- Selection of the internal clock : VME clock ou internal oscillator

The front panel of the Scale32 VME Module can be seen in Figure 12.1 and and the layout of the board can be seen in Figure 12.2. The correct settting of the onboard jumpers can be seen in Table 12.1.

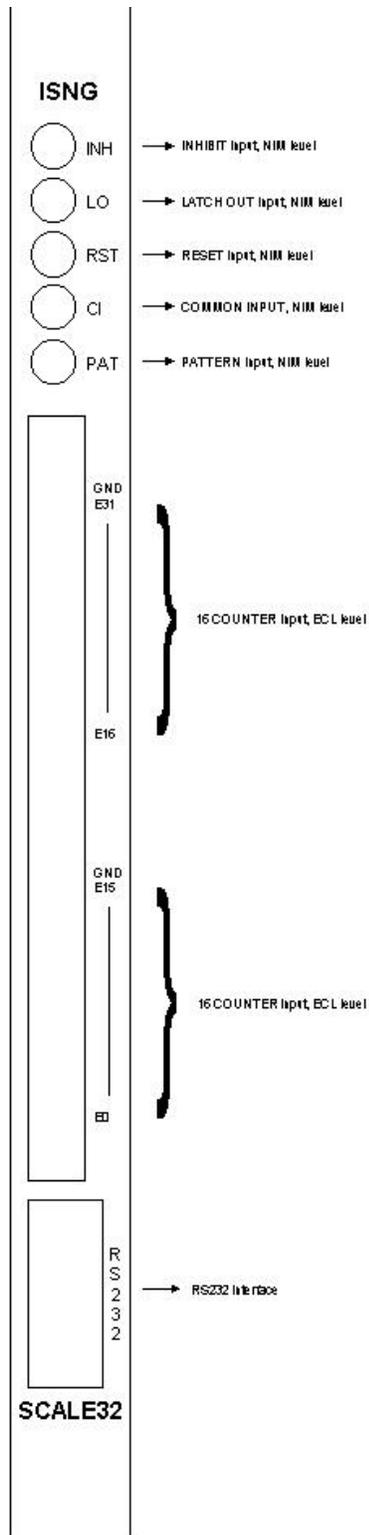


Figure 12.1: Front Panel of the Grenoble Scaler32.

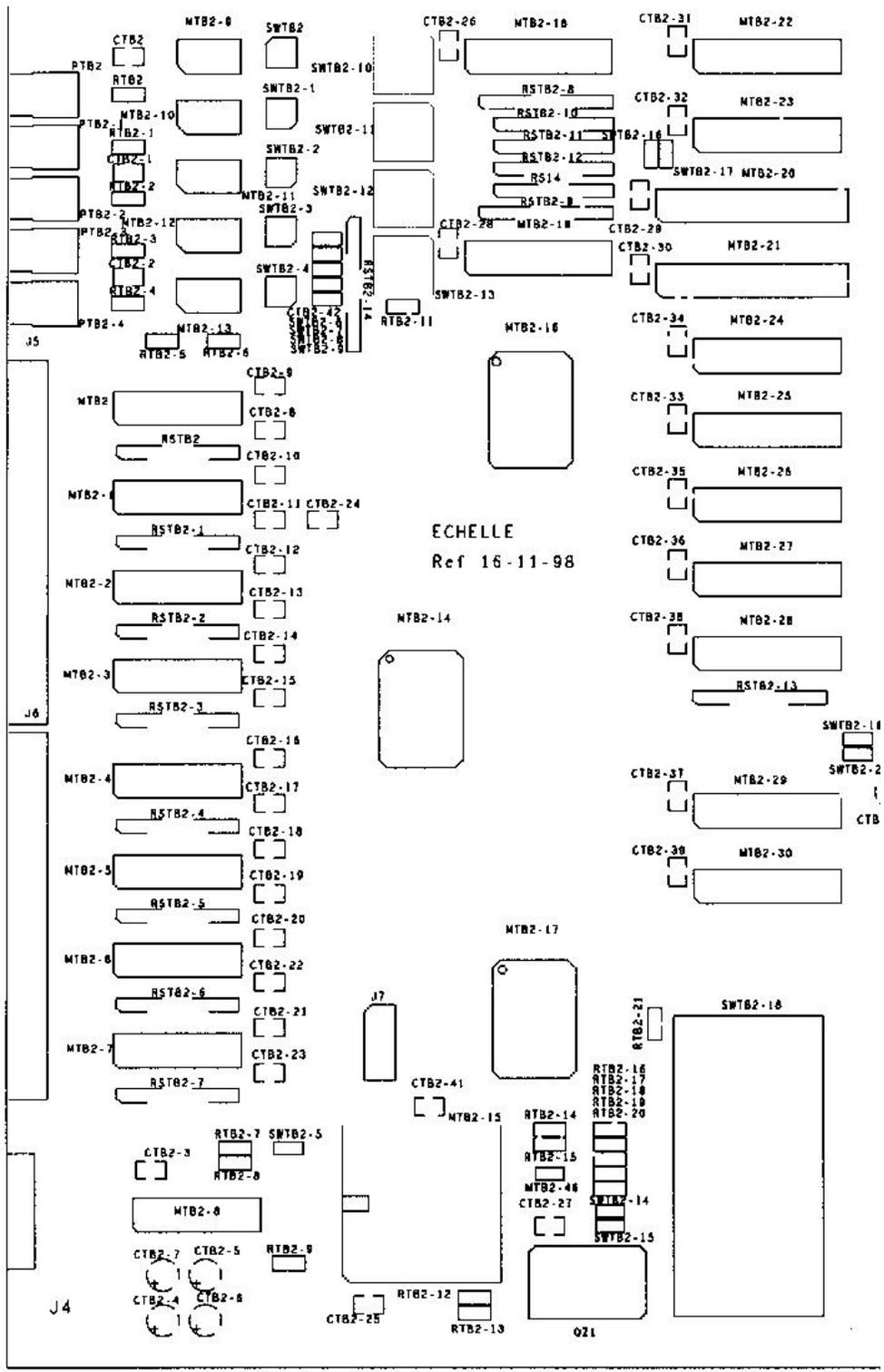


Figure 12.2: Layout of the Scaler32 VME Module.

Jumper	Effect	Setting
SWTB2	?	Down
SWTB2-1	Set's Active State of LATCH	Up
SWTB2-2	Set's Active State of RESET	Down
SWTB2-3	Set's Active State of Common Input (CI)	Up
SWTB2-4	Set's Active State of PAT	Up
SWTB2-14	Set the SCALE clock to be external	Closed
SWTB2-15	Set the SCALE clock to be internal	Open
SWTB2-17	?	Left
SWTB2-19	Set if 5V exists at the backplane	Open
SWTB2-20	Set if 5V doesn't exist at the backplane	Closed
U1	?	Down

Table 12.1: Jumper settings for Scale32 Module. Directions are assuming the board is laying component side up and the front panel is to the left.

# Appendix A

## Power and Crate Requirements

Module	Crate	Voltage	Power	Power Connector
CEBAF	custom 6U high	5 VDC 2 VDC	1.2 W 0.7 W	table 8.2
DADDY	custom 6U high	5 VDC 2 VDC	17.0 W 5.2 W	table 9.1
KGB	custom 6U high	5 VDC 2 VDC	5.0 W 1.5 W	table 4.2
LTD	custom 6U high	5 VDC 2 VDC	14.0 W 7.2 W	table 6.9
SDB	custom 6U high	5 VDC 2 VDC	0.5 W 1.1 W	table 5.1
Meantimer	NIM double wide	+6 VDC 6 VDC 117 VAC	0.8 W 13.2 W 3.5 W	table 3.3
Munger	17" rack			
Splitter	17" rack			

Table A.1: Power and crate requirements for custom electronic boards.

# Appendix B

## Cables and Connections

Connector 1	Con. Type	Connector 2	Con. Type	Type of Cable	Length of Cable	Quantity	Notes
Splitter	34 pin DIN female	ADC	34 pin DIN female	Twisted Pair 34 cond.	160" 8 flats	16	parity reversed at ADC end
CFD	34 pin DIN female	Meantimer TDC	34 pin DIN female	Twisted Pair 34 cond.	140" 7 flats	16	3 connectors, CFD in the middle, 3 flats to MT, 4 flats to TDC.
Meantimer	34 pin DIN female	TDC	34 pin DIN female	Twisted Pair 34 cond.	160" 8 flats	8	
Meantimer	10 pin DIN female	LTD	10 pin DIN female	Twisted Pair 10 cond.	60" 3 flats	32	
LTD	50 pin DIN male	Munger	16 pin DIN female	Twisted Pair 50 cond.	00" 0 flats	32	3 16 pin connectors at Munger end
LTD Buddy	10 pin DIN female	Scaler	34 pin DIN female	Twisted Pair 34 cond.	140" 7 flats	10	4 10 pin connectors at LTD end
LTD Error	Molex female	Scaler	34 pin DIN female	Twisted Pair 34 cond.	140" 7 flats	2	16 Molex connectors at LTD end
Munger	16 pin DIN female	Scaler	34 pin DIN female	Twisted Pair 34 cond.	100" 5 flats	96	2 16 pin connectors at Munger end

Table B.1: A list of all twisted pair cables required for the custom electronics.

Module 1	Module 2	Length	Quantity	Notes
CEBAF	KGB	000" 8 ns	2	CLK and YO
KGB	SDB	000" 13 ns	1	SYNC
KGB	SDB	000" 16 ns	4	CLK with polarity reversed
SDB	SDB	000" 8 ns	4	SYNC
SDB	LTD	000" 8 ns	32	SYNC
SDB	LTD	000" 16 ns	32	CLK

Table B.2: A list of all twinaxial cables required for the custom electronics.

Front Panel Connector	Number of Conductors	Length	Quantity
Input 1	34	0.000"	1
Input 2	34	0.000"	1
TDC output	34	0.000"	1
LTD 1 LTD 4	34	0.000"	2
LTD 2 LTD 3	34	0.000"	2

Table B.3: A list of internal jumper cables required for the meantimer modules. Each cable has a female DIN connector at the printed circuit board end and a male DIN connector at the front panel end.

# Appendix C

## Rack Layout



# Appendix D

## OrCAD files and Diagrams

Board Name	Directory	File Name
CEBAF	C:\ORCAD\G0\CEBAF\	CEBAF.BD1
DADDY	C:\ORCAD\G0\DADDY\	DADDY.BD1
KGB	C:\ORCAD\G0\KGB\	KGB.BD1
LTD	C:\ORCAD\G0\LTD\	LTD.BD1
Meantimer	C:\ORCAD\G0\MEANTIME\	MEANTIME.BD1
Mini-Mungr	C:\ORCAD\G0\MUNGER\	MUNGER.BD1
SDB	C:\ORCAD\G0\SDB\	SDB.BD1
Splitter	C:\ORCAD\G0\SPLITTER\	SPLITTER.BD1

Table D.1: Files currently located in the CMU MEG Physics Machine Room Wean Hall 8423

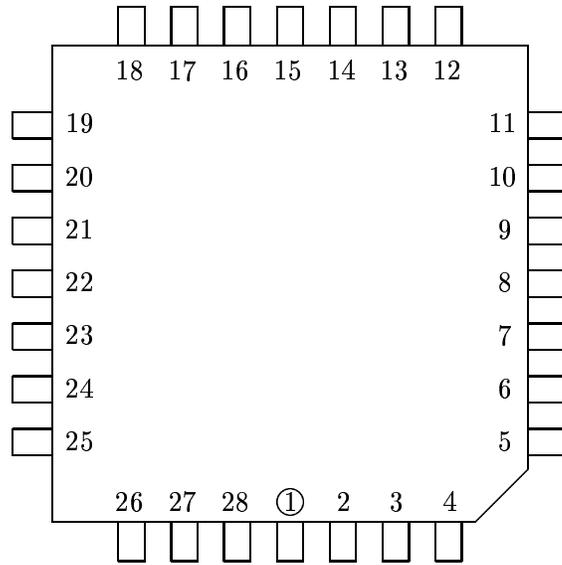


Figure D.1: Top view of a 28 pin PLCC socket.

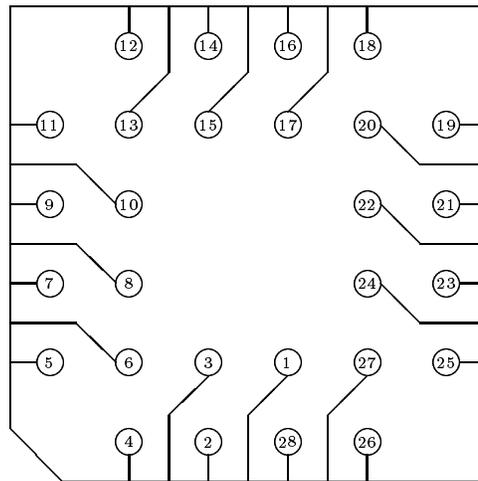


Figure D.2: Bottom view of a 28 pin PLCC socket.

# Appendix E

## Trouble Shooting

Problem	Solution
No data, French or NA	Check CLK and YO signals.
No data, NA only	Check Macropulse gate to KGB. Check KGB outputs with adapter box. Make sure the KGB is producing both a gated CLK train and a SYNC pulse.
Counts in the LTD error scalers	Check the LTD error lights to see which sort of error is occurring: NO SYNC (see below) TOO FEW (see below) TOO MANY (see below)
LTD error lights (NO SYNC)	Check KGB output with adapter box. Make sure the KGB is producing a SYNC pulse. If so, make sure the SDBs are producing copies of SYNC for the LTDs.
LTD error lights (TOO FEW) (TOO MANY)	Flex the CLK and SYNC cables (TOO FEW). Check KGB outputs with adapter box. Make sure the KGB is producing a gated CLK train with 12 pulses. Adjust the KGB parameters as needed.
No data, single LTD channel F.B. ADC channel ok	Check the CFD output.
No data, single LTD channel F.B. TDC channel ok (CFD output)	Check the MT output. If no MT output, check MT input.
No data, single LTD channel F.B. TDC channel ok (MT output)	Check cable from MT output to LTD input. If LTD input is ok, the problem is on the LTD board.
No data, single LTD channel No F.B. data	Check Splitter inputs and outputs. Is there HV on the PMT?
No data, group of 4 LTD channels	Check LTD power lights (green). If they are off, check the circuit breakers on the power distribution panel.
No data, group of 8 LTD channels	Check LTD power lights (green) Check the SDB which provides the CLK and SYNC signals to these channels.
Missing data in one time bin for a single LTD channel	Check Munger input and output cables.
Missing data in 1 time bin for a group of 8 LTD channels	Check Munger output cables.
Missing data in 2 time bins for a group of 8 LTD channels	Check scaler module.
Missing data in 8 time bins for a group of 8 LTD channels	Check Munger input cable.

Table E.1: Potential problems and their potential solutions. Your results may vary.