

G

Electronics
&

Data Acquisition

General introduction

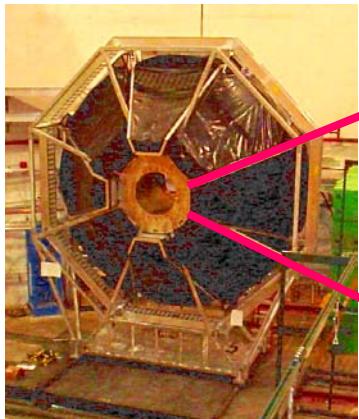
"North American" Electronics

"French" Electronics

Status

Detectors and particles identification

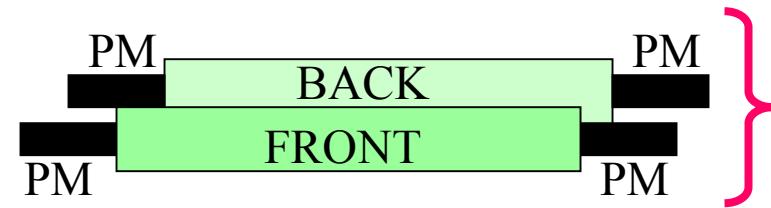
8 sectors (octants)



1 octant



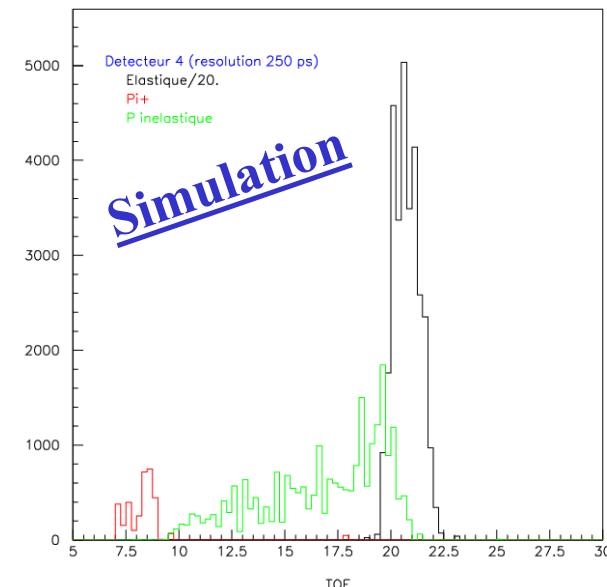
16 pairs of scintillators / octant



→ Total : 512 PMTs

Forward angles : protons

- Front/ Back coincidence
- Identification : TOF
 - START : Beam pick-off (YO)
 - Beam pulse : every 32ns

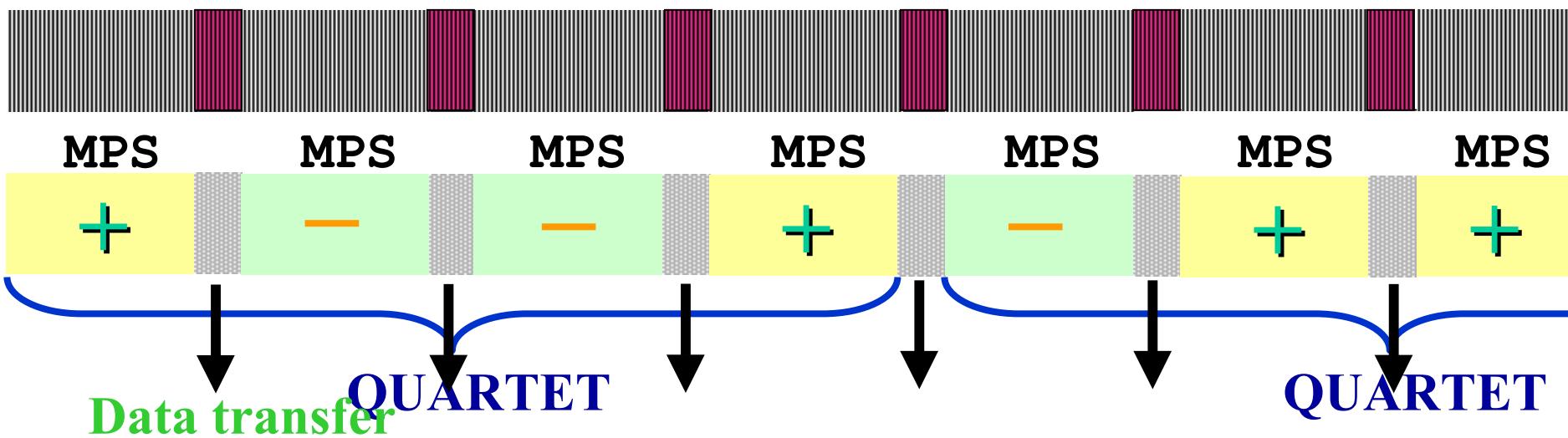




Beam Structure

- YO [START] = **32MHz** ($\text{HF}_{\text{Hall C}} / 16$)
- Helicity is flipped at **30Hz** (every 33ms)
MacroPulse (MPS) : 1 helicity state duration (**33ms**)

Helicity Flip
200 μ s
 \leftrightarrow

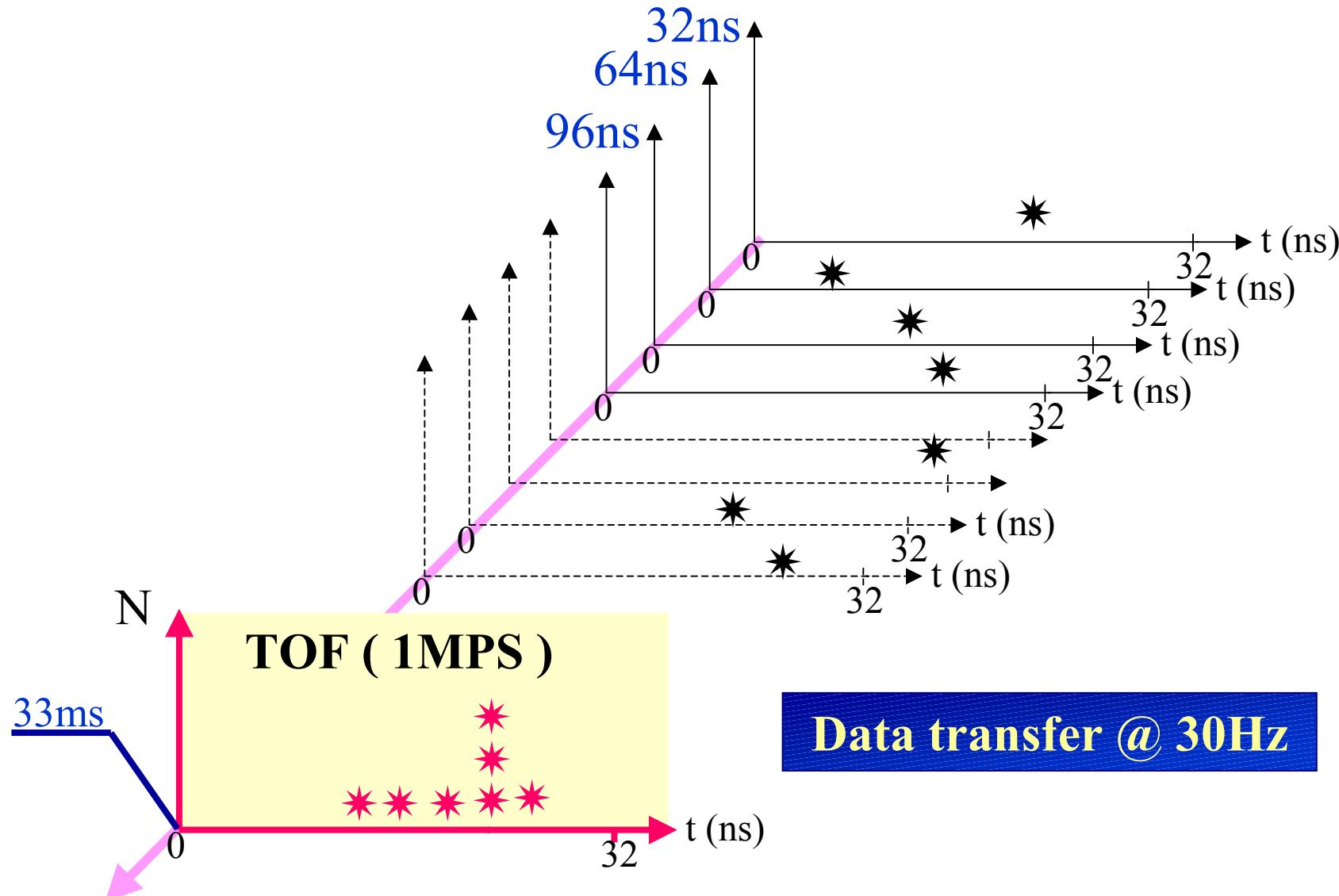


Goal :

Build 1 Histogram (TOF) per MPS



Bin per bin summation
over all beam pulses ($\sim 10^6$) in 1 MPS



Detection :

Events counting

Event rate up to **4 MHz** for each detector (Front/Back coinc.)

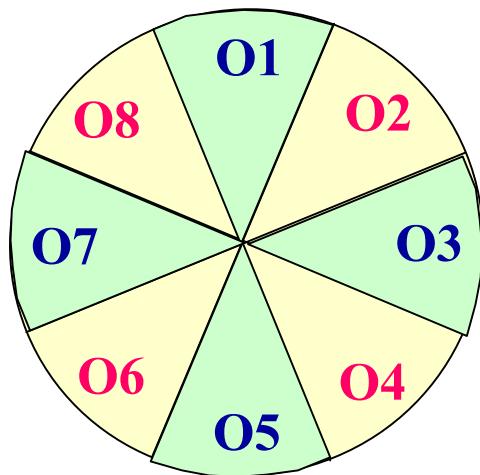
16 x 8 detectors \Rightarrow up to $128 \times 4 \text{ MHz} = \boxed{\textbf{512 MHz}}$ (total)

Data Flux :

Forward angles measurements

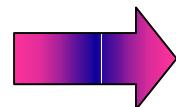
Total Flux : $\sim \textbf{2MB / s}$!

1000h beam time ($3.6 \times 10^6 \text{ s}$) \rightarrow **$\sim 7 \times 10^6 \text{ MB} !!$**



Odd Octant number : " North American"

Even Octant number : " French"

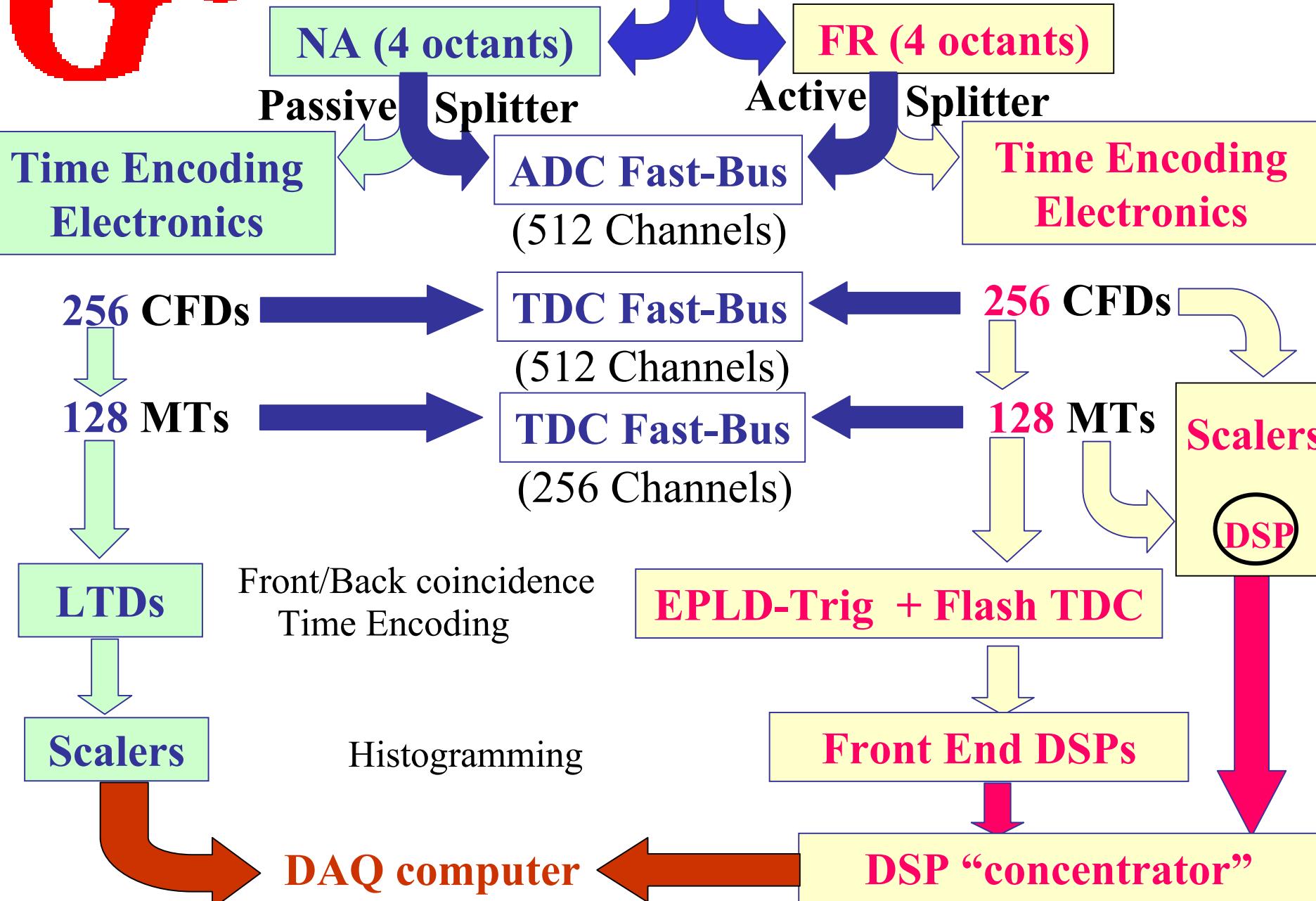


$2 \neq$ electronics designs



512 PMTs Signals

General Scheme

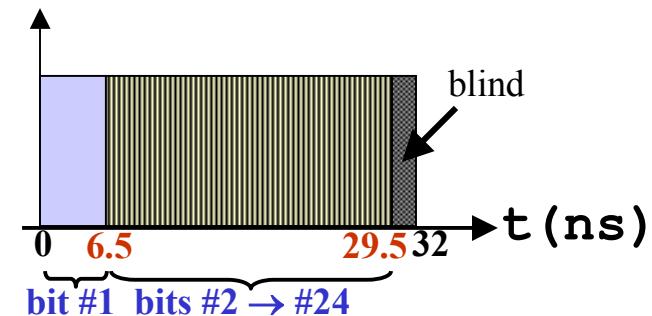
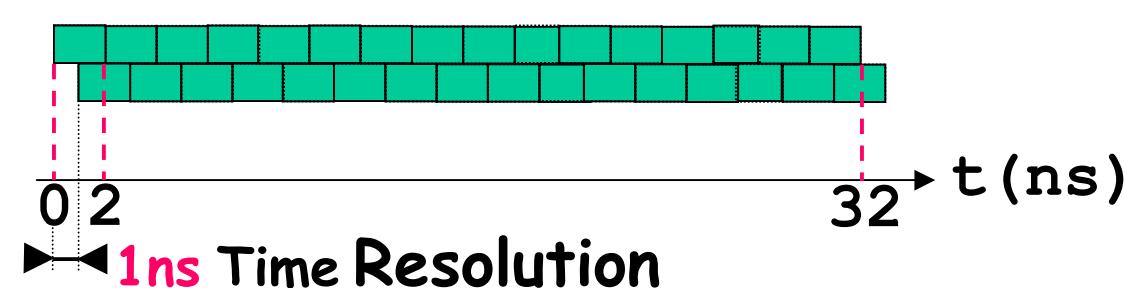


G "North American" Electronics

CFDs (16 channels) : commercial modules

MTs Custom ASICs designed by ISN Grenoble (France)
(Digital) 1 ASIC \Rightarrow 2 MT channels
 8 ASICs / MT board (Carnegie Melon Univ., USA)

LTDs Latching Time Digitizer (Carnegie Melon Univ., USA)
Front / Back Coincidence + Time Encoding
2 16bits Shift Registers (500MHz \Leftrightarrow T=2ns)



Output of LTDs : 24 bits

Scalers VME 32 channels - 100MHz
Custom ASICs designed by **ISN Grenoble (France)**

| | Number of channels/module | Total number of modules |
|---------|---------------------------|-------------------------|
| CFDs | 16 | 16 |
| MTs | 16 | 8 |
| LTDs | 4 MT channels | 32 |
| Mungers | 64 | 8x3 |
| Scalers | 32 | 48 + 3 |

Mostly Custom
&
MODULAR

Advantage of 2 ≠ designs :

Independent cross checks



"French" Electronics

4 OCTANTS 8 DMCH-16X modules

1 DMCH-16X module : **1/2 octant** { **32 Discriminators**
16 Mean-Timers

Highly Integrated Design, Custom,
Very Compact and Software controlled



Discriminators

Mean-Timers

Time Digital Converter

Histogramming

16 channels

X for VXI standard

THE DMCH-16X MODULE

CFD - MT daughter boards (16 / DMCH-16X)

Analogical CFDs & MTs

EPLD-TRIG (4 / DMCH-16X)

Programmable Logical Device

Numerical Flash TDC (2 / DMCH-16X)

Custom ASIC designed in IPN Orsay

250 ps Time Resolution ($128 \times .250 = 32$ ns)

S - DMCH daughter board (1 / DMCH-16X)

“Scalers”

- 1 FPGA chip 104 countings (CFDs & MTs)
- 1 DSP (Digital System Processor)

G - DMCH daughter board (1 / DMCH-16X)

Internal Generator

- 2 time correlated signals (with amplitude variation)
⇒ Test of CFDs thresholds and MT outputs

DSPs (5 / DMCH-16X)

Digital System Processor

- 4 Front End DSPs (Histogramming) / DMCH-16X
- 1 DSP “concentrator” / DMCH-16X

DSP “Concentrator”

Front End DSPs

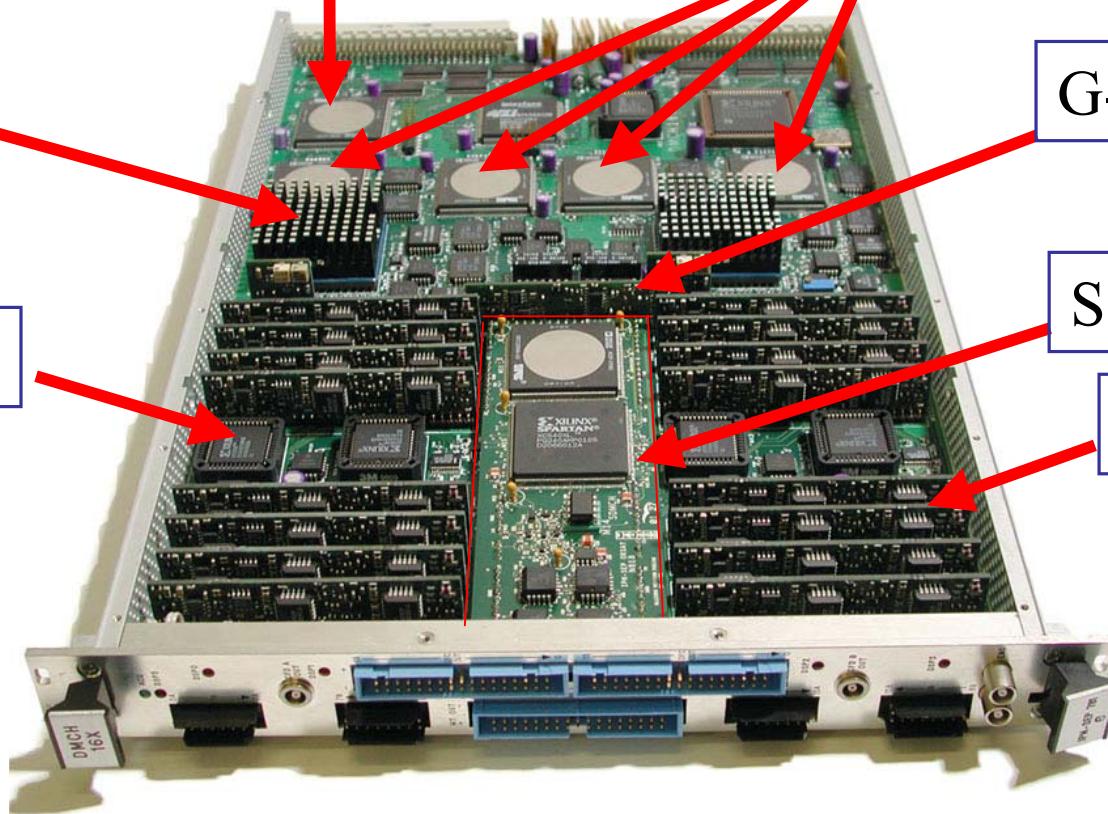
FlashTDC

EPLD-Trig

G-DMCH

S-DMCH

CFD-MT



“The conductor of the French acquisition”

☞ deals with fundamental signals :

- ◆ YO (32 MHz)
- ◆ MPS

☞ permits operational modes :

- ◆ STAND ALONE mode (Test mode)
- ◆ TRIGGERED mode : within the Trigger Supervisor

Some of the software utilities : **OFF-LINE**

- Control of CFDs thresholds(Internal G-DMCH generator)
- TDCs differential linearity Optimization
- Front / Back coincidence Fine Tuning

- NPN : Next (beam) Pulse Neutralization For Dead Time control

After 1 hit in a detector : disable coding during the next beam pulse

- “Buddy” detectors :

For beam stability control and
Dead Time corrections

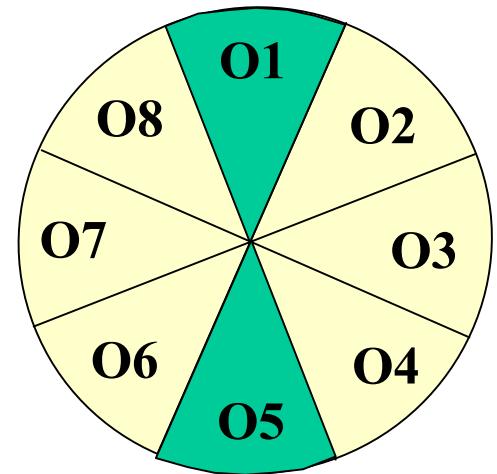
Symmetric to each other at **180°**

Ex : O1D2 and O5D2 are **buddies** to each other

Comparison of event rates in opposite detectors as a means of controlling fluctuations in beam conditions (position, current) and evaluate Dead Time on-line.

- Acquisition @ 120 Hz :

Oversampling of the 30Hz helicity window





Electronics Status

- ✓ Electronics Intrinsic Asymmetry compatible to zero within stat. error
- ✓ ALL modules installed @ JLab
- ✓ DAQ is configured (NA + FR + Fast-Bus + Beam scalers)
Have already taken data using parasitic beam in Hall C
Ready for the commissioning (fall '02)

--> Backward angles measurements :

Detection : electrons
CED/FPD coincidence + Č (e^-/π^- separation)

Electronics :

- FR : 2 additional modules (under tests) ISN Grenoble
- NA : New Design (under tests) Louisiana Tech Univ., USA

G

General Architecture for 1 Detector

